VISHAY INTERTECHNOLOGY, INC.

INTERACTIVE
data book

THIN FILM PRODUCTS
VISHAY ELECTRO-FILMS

VSD-DB0005-0404

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VISHAY INTERTECHNOLOGY, INC.

DATA BOOK

THIN FILM PRODUCTS

Vishay Electro-Films, Inc.

High Density Interconnects

Hybrid Resistors/Capacitors

Microwave Components

Inductors

High TCR Sensors

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VISHAY INTERTECHNOLOGY, INC.

DISCRETE SEMICONDUCTORS	**RECTIFIERS**	Schottky (single, dual)
		Standard, Fast and Ultra-Fast Recovery (single, dual)
		Clamper/Damper
		Bridge
		Superectifier®
		Sinterglass Avalanche Diodes
	SMALL-SIGNAL DIODES	Schottky and Switching (single, dual)
		Tuner/Capacitance (single, dual)
		Bandswitching
		PIN
	ZENER & SUPPRESSOR DIODES	Zener Diodes (single, dual)
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		Dual Gate MOSFETs
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		Custom products
	ICs	Power ICs
		Analog Switches
PASSIVE COMPONENTS	**CAPACITORS**	Tantalum Capacitors
		Solid Tantalum Capacitors
		Wet Tantalum Capacitors
		Ceramic Capacitors
		Multilayer Chip Capacitors
		Disc Capacitors
		Film Capacitors
		Power Capacitors
		Heavy Current Capacitors
		Aluminum Capacitors
		Silicon Capacitors
	RESISTIVE PRODUCTS	Foil Resistors
		Film Resistors
		Thin Film Resistors
		Thick Film Resistors
		Metal Oxide Film Resistors
		Carbon Film Resistors
		Wirewound Resistors
		Variable Resistors
		Cermet Variable Resistors
		Wirewound Variable Resistors
		Conductive Plastic Variable Resistors
		Networks/Arrays
		Non-Linear Resistors
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Not all products listed in this catalog are generally recommended for use in life support systems where a failure or malfunction of the component may directly threaten life or cause injury.

The user of products in such applications assumes all risks of such use and will agree to hold Vishay Intertechnology, Inc. and all the companies whose products are represented in this catalog, harmless against all damages.

- High Density Interconnects
- Hybrid Resistors/Capacitors
- Microwave Components

Vishay Electro-Films, Inc.
Thin Film Technology

- Inductors
- High TCR Sensors

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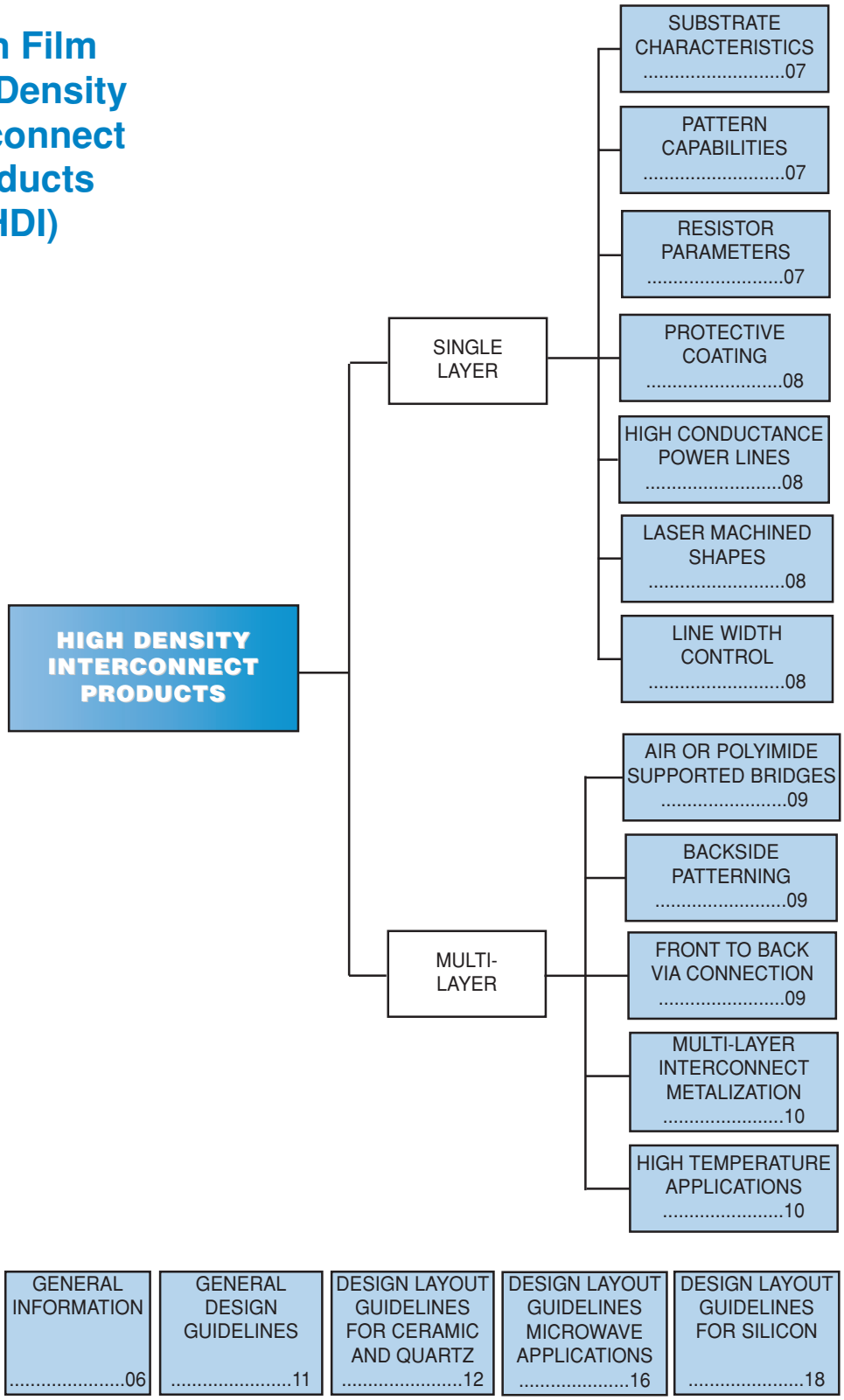
Thin Film High Density Interconnect Products (HDI)



Substrate Design Guidelines Single Layer

Vishay Electro-Films

GENERAL INFORMATION

Vishay Electro-Films (EFI) has produced high quality, patterned thin-film substrates in volume since 1974 for both the hybrid circuit and the microwave industries. These products are used in both military and industrial hybird circuit applications. Our unique volume capability is achieved through the use of high capacity metalizing systems and patterning processes providing tight process parameter control, product uniformity, and production flexibility. This long term experience with engineering and manufacturing of these products has naturally evolved into the expertise necessary to engineer and manufacture high density multi-layer products, flip chip and ball grid array technologies and specific application oriented devices.

Although a high percentage of hybrid or microwave substrates are produced with conductor patterns only, the majority have associated circuit resistors deposited as well. Customers can add active devices and any other passive components as required.

High density and multi-layer products are developed with Vishay EFI and the customer working as a team. Because of the high complexity of these devices and their close relationship to end product performance, this team approach assures the optimum performance and price.

Vishay EFI's processes and equipment have been designed to support the production of small lots as well as high volume runs on the same production and class 1000 lines. All processing is performed in contiguous class 100 clean rooms.

Substrates are available in a wide variety of materials, conductor and adhesion metals and with either nichrome or tantalum nitride resistors depending on the application, customer preference, and manufacturing requirements. Other options include: metalized-through holes, filled vias, backside metalization and patterning, wrap around patterned edges, thick copper power line conductors, and both aluminum and gold wire bond pads on the same substrate to provide monometalic interfaces in very high temperature applications.

- Vishay EFI manufactures patterned substrates for the hybrid circuit industry as large as 4 inches x 4 inches, many with high density fine lines and sometimes with hundreds of resistors.
- Patterning on both surfaces, interconnections by metalized through holes or patterned wrap-around edges.
- Vishay EFI proprietary, military approved, patterned, resistor overcoat protection (required for 0.1% or tighter tolerances). Polyimide available where possible at additional cost.
- Overcoat or polyimide insulation for wire bonding over conductors.
- Special bond pad metalization for very high temperature applications.
- In-house laser machining of specially shaped substrates.
- Beryllium Oxide or Aluminum Nitride substrate material for very high power applications.
- Multi-level metalization using polyimide insulation.

Vishay EFI's high quality is maintained by the extensive use of statistical process controls in league with product assurance teams composed of production, engineering and product assurance personnel. As an added control, 100% of all substrates are visually inspected to MIL-STD-883 Method 2032, level H or K or to the Vishay EFI standard industrial specification as required. 100% of resistors are tested for value and tolerance. Customer-specific inspection and test requirements can also be included.

DESIGN AND LAYOUT

Most customers provide their own layout design, leaving appropriate space for Vishay EFI to design-in the resistors at the proper locations. Vishay EFI guidelines provide the parameters required for calculating the resistor areas as well as design parameters necessary for proper thin film processing and manufacture. After order placement Vishay EFI will design the resistor details and review the layout design sometimes suggesting small modifications to facilitate manufacture.

If required, Vishay EFI can provide the layout design for hybrid substrates from a schematic. In either case the completed layout design is always sent to the customer for final approval prior to mask fabrication.

CAD SYSTEMS

Vishay EFI CAD systems are compatible with DXF and AUTOCAD, thus designs are often received from the customer by direct data link. Additionally, Vishay EFI assembles all resistor probe cards for laser trimming and testing in-house.

This extensive internal production tooling capability enables Vishay EFI to focus on new designs and initial delivery requirements, free from the difficulties that sometimes arise from subcontractor delays.

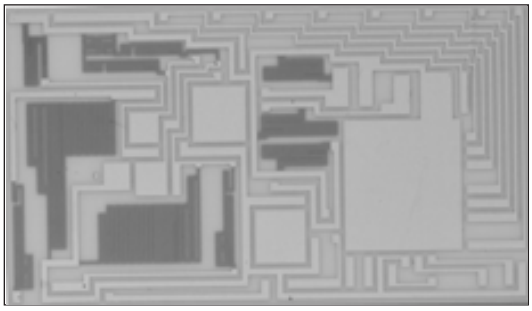
MASK FABRICATION

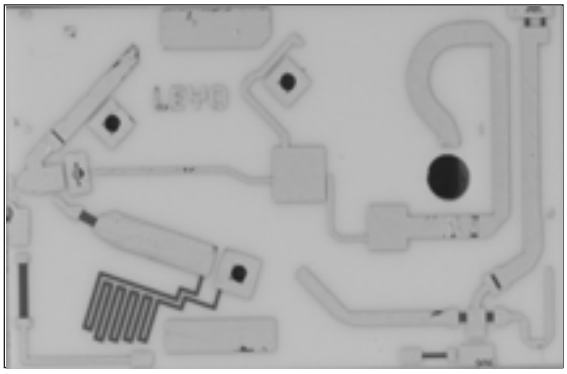
Vishay EFI has masks fabricated by outside vendors. Vishay EFI has developed working arrangements and direct data links with select vendors for quick turn around of mask sets.

PRICE QUOTATION

If your layout is complete, send it with the appropriate data to the Vishay EFI Application Engineering Department (401) 738-9150 FAX: (401) 738-4389. If you do not already have a completed layout, contact our Application Engineers to discuss your requirements. Please include a table of resistor values, tolerances, temperature coefficients of resistance (TCR) and power dissipations.

SUBSTRATE CHARACTERISTICS	
Material	Al_2O_3, BeO, AlN, Quartz, Silicon, Sapphire, Ferrite
Surface Finish Al_2O_3	As Fired, 2µin maximum; Polished, to 0.5µin
Dimensions	0.02 inches x 0.02 inches to 4 inches x 4 inches
Dimensional Tolerance	± 0.005 inches scribed; (± 0.001 inches saw cut)
Thickness	0.005 inches to 0.050 inches
Thickness Tolerance	0.002 inches standard to as tight as 0.0005 inches
Sputtered Resistor	NiCr, Ta_2N
Sputtered Metalization	Ti, TiW, Pd, Ni, Au, Al
Electro-Plated Metals	Au, Cu, Ni, Solder
Electroless Plated	Sn, Ni, Au

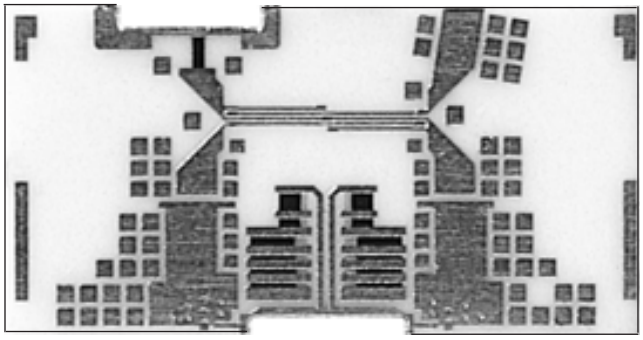




PATTERN CAPABILITIES	
Conductor Line Width	0.002 inches, most economical; 0.001 inches, available
Conductor Line Thickness	50 to 300µinch; 0.002 inches thick Cu standard; up to 0.006 inches available
Line Width Tolerance	0.0001 inch at 150µinches thickness over 2 inch span
Through Hole Minimum Diameter	0.005 inches dependent on substrate thickness
Through Hole Tolerance, Diameter and Position	± 0.002 inches
Metalized Hole Diameter to Substrate Thickness Ratio	0.8 minimum or greater preferred

RESISTOR PARAMETERS	
Value Range	1Ω to 10MΩ
Absolute Tolerance	to ± 0.05%
Ratio Tolerance	to ± 0.01%*
Absolute TCR	± 50ppm/°C standard; ± 25 and ± 10ppm/°C available
Ratio TCR	± 5.0ppm/°C standard; ± 1.0ppm/°C available
Long Term Stability	Absolute and Ratio, see graphs in Resistor Long Term Stability datasheet

*Contact Applications Engineering for tighter tolerances.

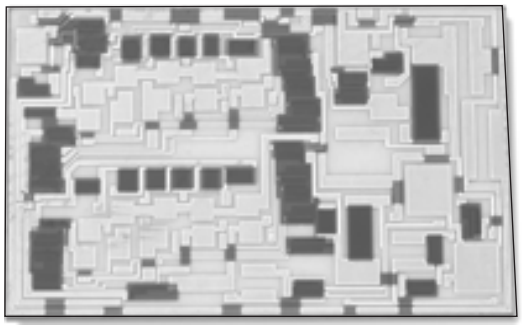


Substrate Design Guidelines Single Layer

Vishay Electro-Films

PROTECTIVE COATING

In 1975, Vishay Electro-Films (EFI) developed a low cost patternable overcoat to protect the resistors and other critical areas from mechanical damage during handling. It is essential to overcoat resistors of 0.1% or tighter tolerances to maintain tolerance during assembly and test of the hybrid, and it is beneficial to overcoat all resistors. This overcoating material was evaluated by the Rome Air Force Development Laboratory and approved for use under MIL-STD-883.

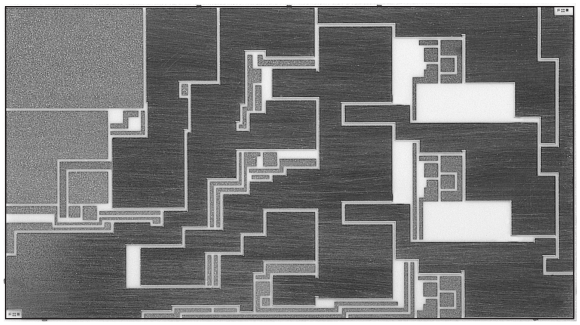


In this photograph the dark areas are where the patterned overcoating has been applied over the resistors.

HIGH CONDUCTANCE POWER LINES

For high power applications, Vishay EFI can provide power lines with up to 0.006 inches thick copper.

Copper conductors to 0.002 inches thickness can be integrated on substrates in relatively close proximity to the fine line patterns without any degradation of the patterning capability.

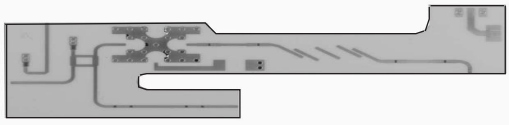


Copper lines are isolated with nickel barrier layers to prevent copper oxidation and intermetalic diffusion during high temperature processing and operation.

This photograph illustrates thick conductor bonding pads and interconnects. Thin small-signal lines can easily be incorporated on the same substrate.

LASER MACHINED SHAPES

In house laser machining of ceramic provides Vishay EFI with the ability to offer custom shaped ceramic substrates, cut outs and holes for special applications.



LINE WIDTH CONTROL

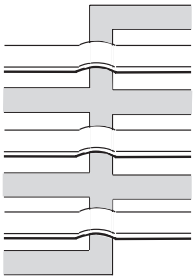
Vishay EFI's tight process controls and extensive class 100 clean room facilities, provide the capability for maintaining superior line width and line edge definition for critical elements such as couplers and filters. Lines of 500 microinches with spaces of 400 microinches and tolerances of ± 50 microinches can be supplied in volume.

Patterned Substrate Products

AIR OR POLYIMIDE SUPPORTED BRIDGES

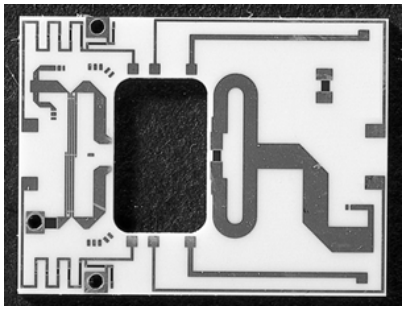
Vishay Electro-Films (EFI) has extensive experience in providing rugged and well-defined air bridges down to 0.001 inch width and with consistent air gap dimensions. The substrate to the right has air bridges associated with the lange coupler section of this microwave circuit.

The line drawing depicts a close up view of the air bridge configuration. The shaded portion of the drawing is the first conductor layer. A sacrificial layer is deposited and patterned before the second conductor layer is put in place. The intermediate layer is then removed leaving the completed air bridge. The same process can be done using polymide; in this case the intermediate polymide layer remains in place on the finished part. Bridges supported by polymide provide a more rugged structure for handling during final hybrid assembly.



LANGE COUPLERS

Combining its fine pattern and supported bridge capabilities, Vishay Electro-Films can offer large coupler features down to 0.5 mil with pattern resolution of 0.1 mil. This type of coupler offers compact design, wide band width and low loss parameters.



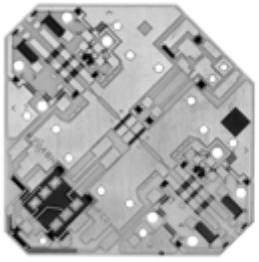
BACKSIDE PATTERNING AND FRONT TO BACK VIA CONNECTION

Conductor interconnect patterns or ground plane definition can be provided on the bottom surface of the substrate. Front to back alignment can be held to 0.003 inches.

The side by side photographs below show the top and bottom conductor patterns of a two-sided patterned substrate. Interconnection from the top and bottom pattern is by metalized through holes.

Front to ground plate or back side conduction pattern connections can be made by metalized through holes, patterned wrap around edges or by means of filled vias. Wherever possible metalized through holes or patterned wrap around edges (or a combination of both) are recommended. The minimum recommended metalized through hole diameter is 80% of the substrate thickness.

The filled via process adds significant complexity and thus cost to the process. Filled vias, however, can be used to provide additional low thermal conductivity paths to a ground plate heat sink where necessary. Vias are planar to 100 microinches.



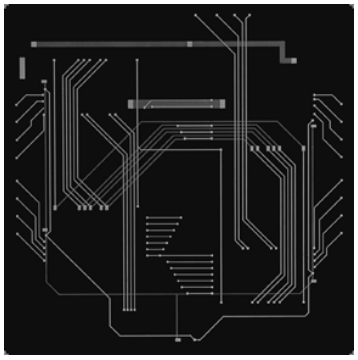
HDI Multi Layer

Vishay Electro-Films

MULTI-LAYER INTERCONNECT METALIZATION

Areas of first level metalization can be overcoated with polyimide and a second level of interconnects can be provided to accommodate high density interconnect requirements.

Two levels of conductors can be seen in areas of the substrate shown to the right. In this case interconnects to the chips on the first layer and to conductors on the first layer are made with wire bonding to the second layer. Interconnects can also be made by metalized through vias.

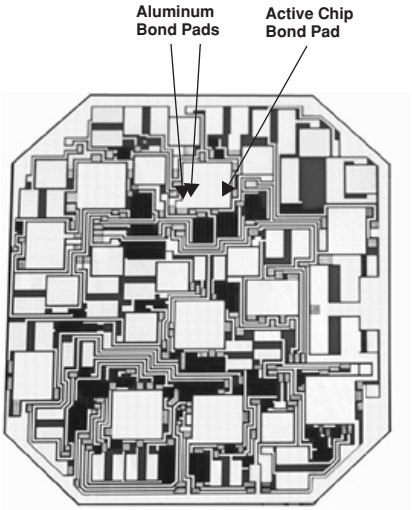


HIGH TEMPERATURE APPLICATIONS

When designing hybrid assemblies to operate at temperatures above 125°C it becomes important to provide monometallic interconnects to prevent intermetalic diffusion and resultant long term reliability problems. For these situations, Vishay Electro-Films (EFI) has developed processes for depositing both aluminum and gold bonding pads on the same substrate. This structure provides for monometallic interconnects. Aluminum wire can be used to connect from the aluminum pads on the substrate. Similarly, gold wire can be used to connect gold pads on the substrate to gold hermetic package terminals. Appropriate barrier metals are included in substrate processing to provide long term reliability in high temperature applications.

Products using this technology have successfully operated at 250°C. The graph on the Resistor Long Term Stability data sheet illustrates stable performance of Vishay EFI nichrome resistors at 200°C operating temperature.

The photgraph to the right shows aluminum bonding pads (light gray) around the active chip bond pad. These aluminum pads are connected to the gold conductor traces with appropriate metallic barrier metalization.



Standard Layout Guidelines

DESIGN CAPABILITIES

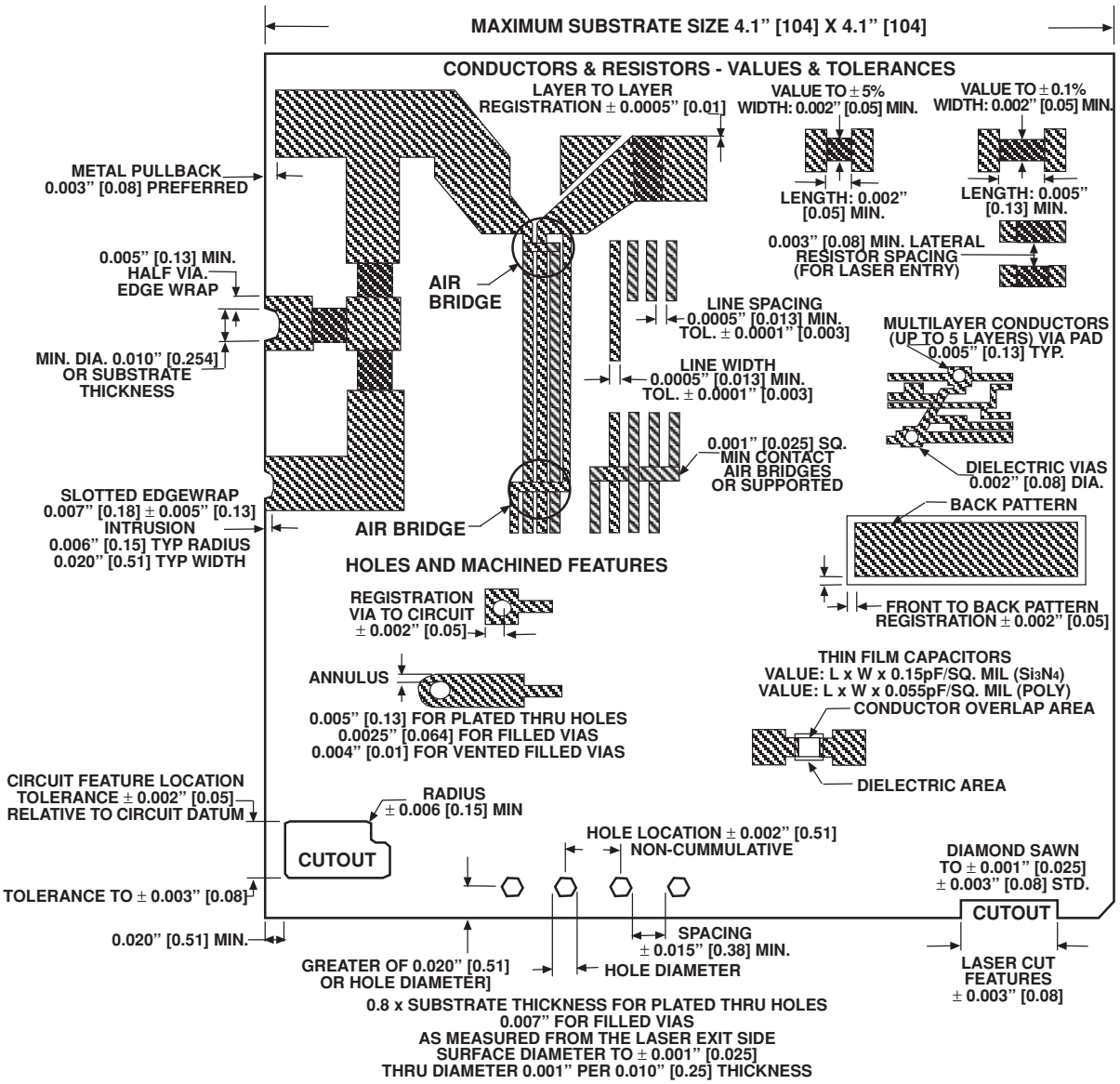
Thin Film High Density Interconnect design guide is directed at engineers looking to design the following:

- Simple resistor networks
- Integrated resistor-capacitor networks
- Multilayer substrate that involve up to 5 layers
- Custom thin film substrate on alumina (Al_2O_3) Aluminum nitride (AlN) or beryllium oxide (BeO)
- Substrates with special shapes, vias, and patterns
- Substrates for microwave applications

The wide array of capabilities allows users to find solutions for applications servicing many markets such as:

- Military
- Automotive
- Instrumentation - microwave
- Telecommunications - CATV, fiber optic and wireless
- Aerospace
- Medical

DIMENSIONS in inches (millimeters)



Design Layout Guidelines for Ceramic Substrates

FOR CERAMIC SUBSTRATES

The following information is the criteria for the layout designer. Deviation from the rules stated below must be done with extreme care. The criteria for the layout designer follows:

1. The maximum active area on a ceramic plate is the nominal size of the plate minus 0.250 inches. Example a 2.00 inches square plate would have an active area of 1.750 inches square.
2. The preferred distance for any conductor, or pad from the substrate border is 0.005 inches. The acceptable distance is 0.002 inches.
3. The preferred conductor line width is 0.004 inches or greater. The preferred space between any two conductors is 0.004 inches. The acceptable distance is 0.002 inches.
4. The preferred probe pad is size 0.010 inches by 0.010 inches. The acceptable probe pad size opening is 0.006 inches by 0.006 inches. The acceptable Kelvin probe pad size opening is 0.008 inches by 0.006 inches. Place probe pads as close to the outside pattern edge as possible, adhering to minimum guidelines, to eliminate probes from shadowing resistors during laser trim.
5. The preferred minimum resistor line width and space 0.001 inches. The acceptable minimum line width and space is 0.0005 inches.
6. The power density at 100Ω/square is 100Watts/inches square at a film temperature of +125°C.
   The current density (I_d), expressed in mA/mil line width, is inversely proportional to the resistivity of the resistor material.

I_d= (k)/ (resistivity) where k=(100)(mA/mil)(ohms/square)

Example (for 25Ω/square);

I_d = [(100)(mA/mil)(Ω/square)/ (25Ω/square)] = 4mA/mil line width

Example (for 50Ω/square):

I_d = [(100)(mA/mil)(Ω/square)/ (50Ω/square)] = 2mA/mil line width

7.0 The optimum resistivity for absolute TCR is listed below:

7.1 For absolute TC of ≤ ± 15ppm/°C use 125Ω/square.

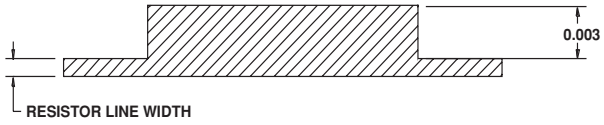
7.2 For absolute TC of > ± 15ppm/°C and ≤ ± 25ppm/°C use 125Ω square (or 100 to 150Ω/square at lower yield).

7.3 For absolute TC of > ± 26ppm/°C and ≤ ± 49ppm/°C use 125Ω/square (or 75 to 175Ω/square at lower yield).

7.4 For absolute TC of ≥ 50ppm/°C the nominal resistivity for design must be within the range of 50 to 200Ω/square.

8.0 Resistors shall be designed using the following criteria:

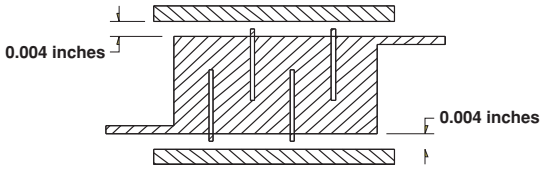
8.1 Any resistor with an absolute tolerance tighter than 0.1% accuracy requires an additional high resolution fine trim area with a minimum trim range of 1% of the nominal value.



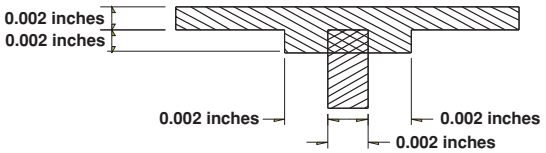
8.2 Design rule for ≥ 150 to 200Ω/square material.
Design to 70% of nominal value with a 70% of nominal trim range.
The 70% trim range may include a 40% trim block, a 20% link and a 10% link.

8.3 Design rule for ≤ 150Ω/square material.
Design to 75% of nominal value with a 60% of nominal trim range.
The 60% trim range may include a 35% trim block, a 15% link and a 10% link.

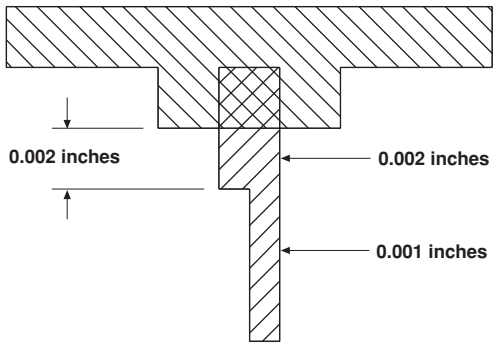
9.0 The preferred spacing between adjacent conductor and resistor is 0.004 inches. The acceptable spacing is 0.002 inches.
The preferred spacing for laser entry and exit is ≥ 0.003 inches between adjacent circuit elements. The minimum spacing is 0.002 inches.



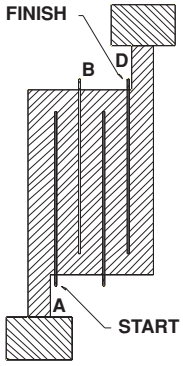
10. Resistor/conductor interface is nominally 0.002 inches. For conductor widths of 0.004 inches or less, the overlap of the resistor termination to the conductor attach area is one-half the conductor width. For conductor widths greater than 0.004 inches, the overlap of the resistor termination to the conductor attach area is one-half the conductor width up to a maximum of 0.005 inches.

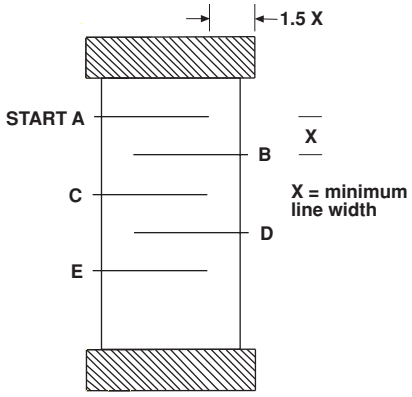


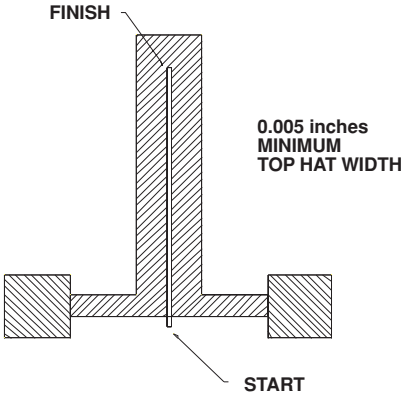
11. Resistor line widths of less than 0.002 inches require a “step-up” to 0.002 inches at the conductor/resistor interface.



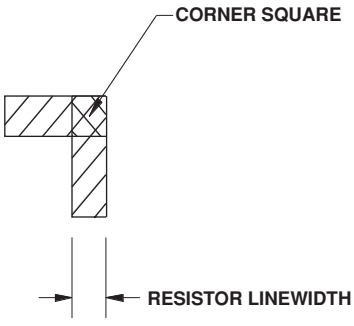
12. Typical designs for trim are as follows:







1. The corner square is considered to be 0.5 squares.



Guidelines: Ceramic

Vishay Electro-Films

DESIGN LAYOUT GUIDELINES FOR CERAMIC SUBSTRATES in inches		
BONDING PADS	**QUARTZ**	**ALUMINA**
Minimum Bonding pads with no overcoat	0.006 x 0.006	0.006 x 0.006
Minimum Bonding pads with overcoat	0.008 x 0.008	0.008 x 0.008
Preferred Bonding pads size	0.010 x 0.010	0.010 x 0.010
Minimum distance from conductor or pad to substrate border	0.002	0.003
Preferred distance from conductor or pad to substrate border	0.003	0.005
RESISTOR TO CONDUCTOR INSERTION		
Resistor to conductor edge	0.001	0.001
Preferred resistor to conductor edge	0.002	0.002
Resistor to conductor insertion	0.002	0.002
Preferred resistor to conductor insertion	(0.003 inches or 50% of attached pad width)	
Resistor line width of less than 2.0 require a step-up	0.002	0.002
MINIMUM SPACING		
Resistor to conductor or pad	0.001	0.0025
Preferred distance from resistor to conductor or pad	0.002	0.004
Resistor to resistor (same resistor)	(same space as resistor linewidth)	
Resistor to resistor (adjacent resistor)	0.0005	0.001
Conductor to conductor	0.001	0.002
Preferred conductor to conductor	0.002	0.004
Distance from resistor to substrate border	0.003	0.005
Preferred distance from resistor to substrate border	0.004	0.007
MINIMUM DIMENSIONS		
Conductor width traces	0.001	0.002
Preferred conductor width	0.002	0.004
Resistor width	0.005	0.005
Preferred resistor width	(0.001 or greater)	
Laser entry	0.002	0.0025
Preferred laser entry	0.003	0.003
Laser kerf width	0.005	0.005
Laser kerf (customer specification)	(Per customer specs.)	
Top hat width	0.003	0.005
Saw cut street width	0.006	0.006
Overcoat distance from the insertion point of the resistor	0.002	0.002
Overcoat covering overlap	0.002	0.002

Notes:

- Pad one must be shaped with a notch or a rounded corner.
- All drawings must show where to measure linewidths.
- All designs must have an alignment marker.
- The corner square on a resistor is considered to be 0.5 squares.
- Any resistor with a tolerance tighter than 0.1% accuracy requires an additional high resolution fine trim area with a minimum trim range of 1% of the nominal value.
- The active area on herman ceramic plate is 4.16 inches by 3.36 inches.
- The active area on super herman ceramic plate is 4.16 inches by 4.16 inches.
- The active area on quartz plate is 2.75 inches by 2.75 inches.

DESIGN LAYOUT GUIDELINES FOR CERAMIC CHIP COMPONENTS in inches	
BONDING PADS	**ALUMINA**
NON-KELVIN	0.004 x 0.004
KELVIN-(R < 1kΩ) or (R < 100kΩ & TOL. < 1%)	0.004 x 0.007
MINIMUM SPACING	
Resistor to Bonding Pad	0.0007
Resistor to Metal	0.0006
Resistor to Resistor (same resistor)	(smaller of resistor width or 0.0005)
Resistor to Resistor (adjacent resistor)	0.0005
Metal to Metal	0.001
MINIMUM OVERLAP	
Metal to Oxide Window	N/A
Metal to Back Contact	N/A
Resistor to Back Contact	N/A
Resistor to Metal	Resistor Continuous under Metal Edges of Resistor & Metal Coincide
MINIMUM DIMENSIONS	
Aluminum width	0.0005
Gold width	0.002
Resistor width	0.0005
Resistor to Metal Connections	0.0005
Ladder Rung width	0.0005
Ladder Gap width	0.0015
Back Contact Window	N/A
Street width	0.008
Ladder Centers (nicking allowed)	2 x RUNG WIDTH
Ladder Centers (no nicking allowed)	RUNG WIDTH + 1.5
Solid Trim	Allowed
5 x Power Density - Conservative	500W/square inches
5 x Power Density - Maximum	5kW/square inch

Notes:

- If possible one Kelvin pad should be on all designs for edge sensing.
- One bonding pad should be shaped differently for orientation purposes.
- All drawings will show where to measure linewidth and its value for critical applications.
- Laser entries will be 0.0015 square inches minimum.
- Overcoat opening shall include street and alignment marker.

Guidelines: Microwave

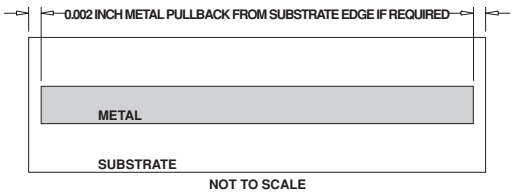
Vishay Electro-Films

Design Layout Guidelines for Microwave Applications

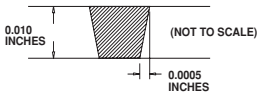
The following guidelines for thin film substrate design are presented to provide the microwave designer with practical and production achievable thin film parameter capabilities as well as to provide a relative cost impact to achieve the tightest specifications. This cost relation is indicated by providing two achievable limits: one with little or no cost premium and the other at some level of cost impact.

The tightest tolerances should be specified only where required for circuit performance. If the tightest tolerances are specified for all parameters, even if not required, unnecessary costs will result.

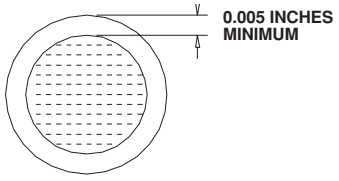
1. **SUBSTRATE SIZE:**
   Sizes are available in most substrate materials to 4 inches x 4 inches. Size tolerances:
   A. Scribe and break ± 0.003 inches most economical
   B. Saw to size ± 0.001 inches small premium
   Surface finish:
   A. 2 - 4 microinch as fired most economical
   B. 2 microinch or 1 microinch maximum polished small premium
   Thickness tolerance as fired:
   A. 0.015 ± 0.002 inches (standard), ± 0.001 inches small premium
   B. 0.010 ± 0.001 inches (standard), ± 0.0005 inches premium
   Thickness tolerance polished:
   A. ± 0.0005 inches standard
2. **METALIZATION:**
   A. Sputtered:
   NiCr, Ta_2N, TiW, Ni, Au, Pd, Al,
   B. Electro- Plated :
   Au (to 500 microinches), Ni (to 200 microinches), Cu (to 0.005 inches). (Thick copper can be selectively plated on the power lines).
   Compatibility: While the majority of these materials can be used in multilayer combinations, some combinations are not compatible dependent on patterning requirements.
   For combinations not widely used or when in doubt, please contact Vishay Electro-Films (EFI) application engineering before finalizing specifications.
3. **PATTERNS:**
   A. Minimum Line Widths or Spaces: 0.0005 inches
   B. Line Width Tolerance:
   a. Metal thickness up to 150 microinches ± 0.0001 inches (standard) ± 0.00005 inches (premium)
   b. Metal thickness over 150 microinches ± 0.0001 inches per each 100 microinches thickness:
   Tighter per discussion with Vishay EFI application engineering (premium).
   C. Metalization to Substrate Edge:
   If metalization is brought to the substrate edge, slight disturbance of the metal will occur because of the sawing or scribing operation. If this slight disturbance is not acceptable, a 0.002 inch designed pullback from the edge is required. This also applies to the backside groundplane.



4. **AIR BRIDGES:**
   Width:
   0.001 inch minimum (standard); 0.005 inch (premium); (either true air bridge or over polyimide dielectric).
5. **THROUGH HOLES:**
   A. Diameter:
   0.006 inch minimum
   B. Taper
   The hole will be tapered down from the laser spot entry side, normally the top side, 0.001 inch for every 0.010 inches substrate thickness. The smallest diameter will be used for the hole dimension.



   C. Patterned Metalized Slits:
   Two slits, 0.002 inches wide and 0.006 inches long, will be placed typically 180° opposite across the rim of the via. They will not be placed in a signal path unless there is no option.
6. **METALIZED THROUGH HOLES:**
   A. Patterns:
   When designing through hole patterns, design aminimum of a 0.005 inches ring around each hole (see figure below) to allow for the tolerance build-up caused by hole placement, manufacturing alignment, diameter tolerance, slight laser entrance hole rounding and other factors.



If this presents a severe design problem, contact Vishay EFI application engineering.

METALIZED THROUGH HOLES (continued)

B. Double Sided, Front to Back Alignment:
± 0.002 inch (standard), tighter, consult Vishay EFI Application Engineering (premium).

C. Metalization:
The same metalization layers should be used on each side of the substrate when metalized through holes are used. (Plating thickness may be different). For example, if resistor material is required on the top side, it should also be used on the bottom side for the adhesion layer.

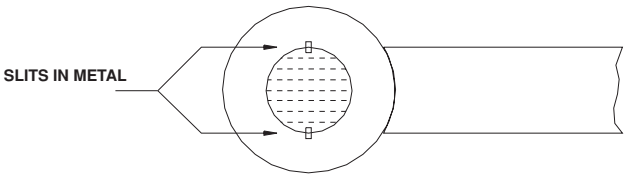
D. Size:
Metalized through hole diameters should have a minimum ratio of 0.8 with substrate thickness.

7. **FILLED VIAS:**

A. Diameter 0.007 inch standard. Center to center hole placement is 0.000015 inch minimum.
Surface finish: The substrate will normally be supplied with a polished or lapped surface necessitated by the fill process.

B. Planarity:
The filled via will not extend above the substrate or be recessed below the substrate by more than 500µin

C. Patterned Metalization Slits:
Two slits, 0.002 inch wide and 0.006 inch long, will be placed typically 180° opposite across the rim of the via. They will not be placed in a signal path unless there is no option.



Hermeticity: Non-Hermetic.

8. **RESISTORS**

A. Material:
Resistors can be either nichrome or tantalum nitride. For most microwave applications tantalum nitride is recommended unless unusual tolerances or long term stability requirements exist.

B. Resistivity:
Recommended resistivity for Ta_2N is 25 -100 ohms/square; for NiCr is 25 - 200 ohms/square.

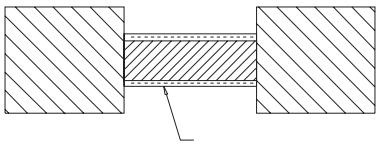
C. Temperature Coefficient:

a. For Ta_2N, 25 - 50 ohms/square, less than ±100ppm/°C; 51-100 ohms/square less than ±150ppm/°C.

b. For NiCr, 25 - 200 ohm/square, less than ± 50ppm/°C.

D. Design:

a. Value:
For Ta_2N, Vishay EFI recommends that all resistors be designed to 80% of value with 20% trim range (e.g. block resistors, add 20% to the width.) All high frequency resistors will be laser edge trimmed to value to preserve frequency response (see figure below). However, Vishay EFI can supply resistors of 20% standard (10% on demand) or looser tolerance which are designed to 100% of value with no laser trimming. Matching of identically designed resistors in relatively close proximity, can be held to 3% without trimming. For nichrome resistors, design all resistors to 80% of value with a 20% trim range.



Resistor laser trimmed around center line to maintain frequency response

b. Power:
To insure adequate long term stability, the following guidelines should be used relative to power handling (current density).

RESISTIVITY (OHMS/SQUARE)	CURRENT/0.001 INCH OF LINE WIDTH
25	4mA
50	2mA
100	1mA
200	0.5mA

E. Stabilization Temperature:
For the best long term stability, all Ta_2N resistors should be stabilized at approximately 425°C. However, please note that if nickel has been specified under gold for solderability, temperatures above 350°C will cause the nickel to diffuse into the the gold creating two problems. One, nickel oxide will form on the gold surface making soldering difficult and secondly, the resistivity of the gold will increase perhaps adversely effecting electrical performance. Specifying palladium in place of nickel will reduce but not eliminate the problem.
For most microwave applications where the resistor tolerances are (Ta_2N) 10% or greater, a stabilization temperature of 350°C, nominal, should provide adequate long term stability, Remember that if the resistors are designed to 100% value with no trim allowed, some range in stabilization temperature is required to provide low cost yields. In no case is it recommended that the stabilization temperature be less than 300°C.

Guidelines: Silicon

Vishay Electro-Films

Design Layout Guidelines for Silicon Substrates

FOR SILICON SUBSTRATES

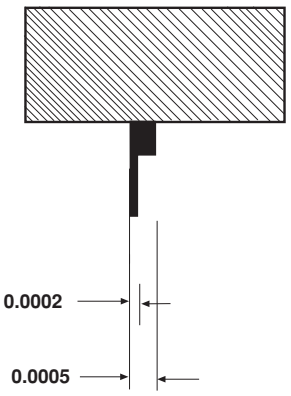
The following information is the criteria for the layout designer.

Deviation from the rules stated below must be done with extreme care. The criteria for the layout designer follows:

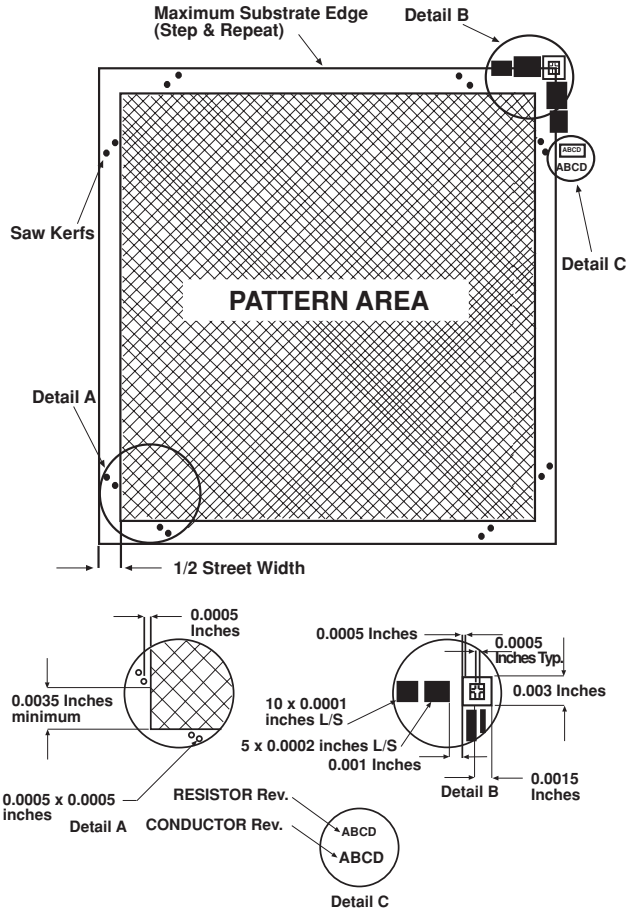
1. The standard wafer dimensions are 3 inches or 5 inches.
2. The minimum spacing of any metal pad to the finished substrate edge is 0.001 inches.
3. The minimum line width and space for any resistive material is 0.00015 inches.
4. The line width for any aluminum conductor is > 0.0005 inches, line width for gold conductor is > 0.001.
5. The minimum bond pad size is 0.008 inches x 0.005 inches. With the 0.008 inches along the edge of the substrate, unless otherwise specified.
6. The power density for silicon is 2500 watts/inches square at 100 ohms per square. The current density (T) expressed in mA/mil is inversely proportional to the resistivity of the resistor material.
   Examples for various sheet resistivities:

25 ohms/square	10000 Watts/inches square	14.14 A/inches	14.14 mA/milinches
50 ohms/square	5000 Watts/inches square	7.07 A/inches	7.07 mA/milinches
100 ohms/square	2500 Watts/inches square	3.53 A/inches	3.53 mA/milinches
200 ohms/square	1250 Watts/inches square	1.75 A/inches	1.75 mA/milinches

7. All resistors with a ratio tolerance of ≤ 0.01% that cannot be designed using a link design will require a solid trim tab capable of providing a trim resolution of 25% of the required tolerance.
8. All resistor line widths that are smaller than 0.0005 inches will require a “step-up” to 0.0005 inches at the resistor/ conductor interface.



9. Laser entries require 0.0015 inches square minimum.
10. Design rule percentages for all parts are as follows:
    Design to 70% of nominal value with a trim range of 70% of nominal trim range (preferred)
    Design to 70 % of nominal value with a trim range of 60% of nominal trim range (acceptable)
11. Minimum spacing between metal and resistor is ≥ 0.001 inches.
12. Spacing between resistor to resistor (adjacent resistor) is 0.0005 inches.
    Spacing between resistor to resistor (same resistor) is the smaller of the resistor width or 0.0005 inches.
13. If overcoat is required it must overlap all bond pads by 0.00025 inches. The street must be free of overcoat material.
14. Most silicon parts require saw kerf marks, made of resistor material, which are placed in the street. These saw kerfs are usually placed on all four corners of substrate. They are placed approximately 0.0005 inches away from the bond pad. All silicon parts require an alignment marker on the upper right corner of the substrate street (see illustration)

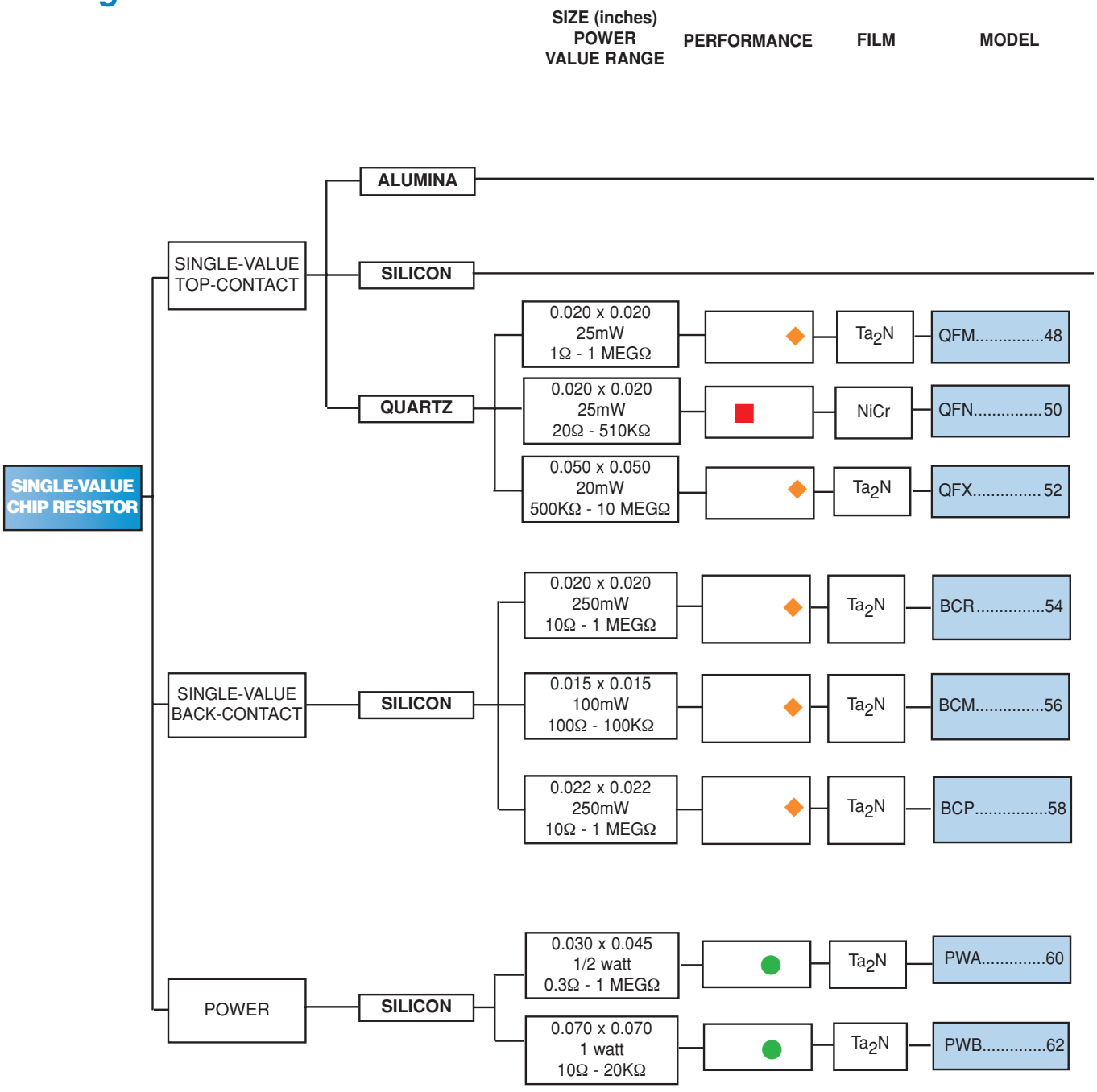


DESIGN LAYOUT GUIDELINES FOR SILICON SUBSTRATES/CHIP COMPONENTS in inches			
BONDING PADS	**SILICON**	**QUARTZ**	**ALUMINA**
NON-KELVIN	0.004 x 0.004	0.004 x 0.004	0.004 x 0.004
KELVIN-(R < 1k ohm) or (R < 100k ohm & TOL. < 1%)	0.004 x 0.007	0.004 x 0.007	0.004 x 0.007
MINIMUM SPACING			
Resistor to Bonding Pad	0.0007	0.0007	0.0007
Resistor to Metal	0.0006	0.0006	0.0006
Resistor to Resistor (same resistor)	(smaller of resistor width or 0.0005)		
Resistor to Resistor (adjacent resistor)	0.0005	0.0005	0.0005
Metal to Metal	0.001	0.001	0.001
MINIMUM OVERLAP			
Metal to Oxide Window	0.0005	N/A	N/A
Metal to Back Contact	0.0005	N/A	N/A
Resistor to Back Contact	0.0005	N/A	N/A
Resistor to Metal	Resistor Continuous under Metal Edges of Resistor & Metal Coincide		
MINIMUM DIMENSIONS			
Aluminum width	0.0005	0.0005	0.0005
Gold width	0.001	0.001	0.002
Resistor width	0.0001	0.0001	0.0005
Resistor to Metal Connections	0.00025	0.00025	0.0005
Ladder Rung width	0.0002	0.0002	0.0005
Ladder Gap width	0.0015	0.0015	0.0015
Back Contact Window	0.003 x 0.003	N/A	N/A
Street width	0.006	0.008	0.008
Ladder Centers (nicking allowed)	2 x RUNG WIDTH		
Ladder Centers (no nicking allowed)	RUNG WIDTH + 0.0015		
Solid Trim	Not Preferred	Not Preferred	Allowed
5 x Power Density - Conservative at 50Ω/square	25kW/square inches	200W/square inches	500W/square inches
5 x Power Density - Maximum*	50kW/square inches	2.5kW/square inches	5kW/square inches

Notes

- If possible one Kelvin pad should be on all designs for edge sensing.
- One bonding pad should be shaped differently for orientation purposes.
- All drawings will show where to measure line width and its value for critical applications.
- Laser entries will be 0.0015 square inches minimum.
- Overcoat opening shall include street and alignment marker.
- Maximum ratings degrade long term drift characteristics.

Thin Film Chip Resistors Wire Bondable Single Value



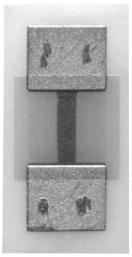
SIZE (inch) POWER VALUE RANGE	PERFORMANCE	FILM	MODEL
0.020 x 0.040 40mW 10Ω - 24KΩ	■	NiCr	CC1.....22
0.030 x 0.030 40 mW 25Ω - 40KΩ	▲	NiCr	CC2.....24
0.050 x 0.050 100mW 30Ω - 125KΩ	▲	NiCr	CC3.....26
0.050 x 0.0100 175mW 50Ω - 400KΩ	▲	NiCr	CC4.....28
0.100 x 0.100 400mW 45Ω - 1 MEGΩ	▲	NiCr	CC5 30
0.030 x 0.045 65mW 20Ω -59KΩ	▲	NiCr	CC6.....32
0.020 x 0.020 40mW 20Ω - 10KΩ	●	NiCr	CC8.....34
0.020 x 0.020 50mW 10Ω - 10KΩ	◆	Ta_2N	SFC.....36

SIZE (inches) POWER VALUE RANGE	PERFORMANCE	FILM	MODEL
0.020 x 0.020 250mW 1Ω - 1 MEG Ω	■	Ta_2N	SFM.....38
	■	Ta_2N	SFP.....40
0.020 x 0.020 125mW 20Ω - 510KΩ	▲	NiCr	SFN.....42
0.040 x 0.040 20mW 510KΩ - 20 MEGΩ	◆	Ta_2N	SFX.....44
0.050 x 0.050 400mW 100Ω - 50KΩ	■	NiCr	SC3.....46

Performance Key

▲	■	●	◆
TCR ± 10ppm/°C TOL ± 0.05%	TCR ± 25ppm/°C TOL ± 0.1%	TCR ± 50ppm/°C TOL ± 0.5%	TCR ± 100ppm/°C TOL ± 1%

Thin Film 0402 Size Resistor on Alumina



Product may not be to scale

FEATURES

- Small single chip size: 0.020 x 0.040 inches
- Resistance range: 10Ω to 24kΩ
- Alumina substrate
- Low stray capacitance: < 0.2pF
- Resistor material: nichrome
- Resistor passivation coat optional
- Solder Pads optional

The CC1 series single-value resistor chips offer a small size, low shunt capacitance and solder pad option. The CC1s nichrome resistor material offers excellent stability.
The CC1s are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CC1s are 100% electrically tested and visually inspected to MIL-STD-883.

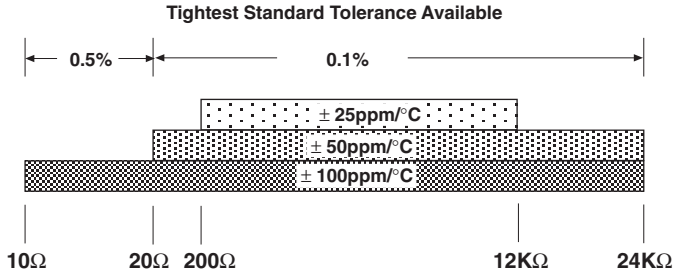
APPLICATIONS

Vishay EFI CC1 chip resistors provide excellent high-frequency response and are ideally suited for prototyping.
Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

Recommended for hermetic environments where die is not exposed to moisture.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES* AND TOLERANCES



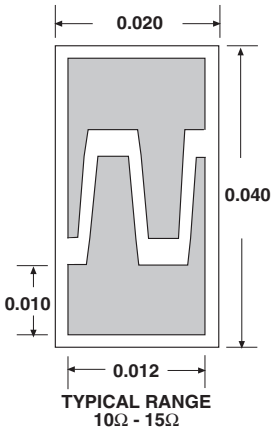
Note*
Only 25Ω to 1kΩ are standard strip line designs for microwave applications

STANDARD ELECTRICAL SPECIFICATIONS

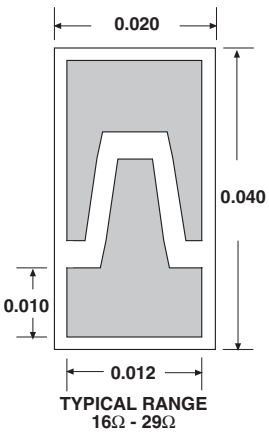
PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Moisture resistance, MIL-STD-202 Method 106 - Hermetic applications	± 0.2% maximum ΔR/R
Stability, 1000 hours, + 125°C, 40mW	± 0.1% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.1% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 125°C (derated to zero at + 150°C)	40mW maximum
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

VISHAY ELECTRO-FILMS • FRANCE +33.4.93.37.28.24 FAX: +33.4.93.37.27.31 • GERMANY +49.9287.710 FAX: +49 9287.70435 • ISRAEL +972.3.557.0945 FAX: +972.3.558.9121
• ITALY + 39.2.300.11911 FAX: +39.2.300.11999 • JAPAN +81.3.5464.6411 FAX: +81.3.5464.6433 • SINGAPORE +65.788.6668 FAX: +65.788.0988
• SWEDEN +46.8.594.70590 FAX: +46.8.594.70581 • UK +44 191 514 8237 FAX: +44 1953 457 722 • USA: (401) 738-9150 FAX: (401) 738-4389

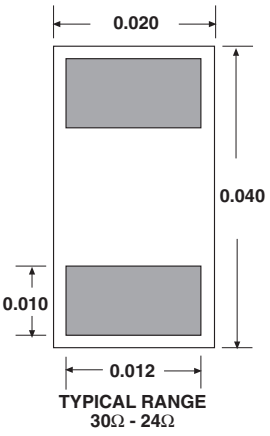
DIMENSIONS in inches



TYPICAL RANGE
10Ω - 15Ω



TYPICAL RANGE
16Ω - 29Ω



TYPICAL RANGE
30Ω - 24Ω

SCHEMATIC

MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip size	0.020 x 0.040 ± 0.003 (0.5 x 1.0 ± 0.08mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.03mm)
Chip substrate material	99.6% alumina, 2-4 µinch finish
Resistor material	Nichrome
Bonding pad size	0.010 x 0.012 (0.175 x 0.30mm)
Number of pads	2
Pad material	25kÅ minimum gold standard
Backing	None

OPTIONS: Terminations: Aluminum, Nickel solder (62/32)
Gold back for solder die attach
Contact Applications Engineer

ORDERING INFORMATION

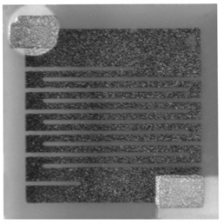
Example: 100% visual, 50Ω, ± 10%, ± 100ppm/°C TCR, Gold Terminations

W	**CC1**	**5000**	**B**	**K**	**E**	**G**
INSPECTION /PACKAGING	PRODUCT FAMILY	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE	TCR	TERMINATIONS
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)		Use first 4 significant digits of resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100	**B** = 0.1%* **C** = 0.25%* **D** = 0.5% **F** = 1.0% **G** = 2.0% **J** = 5.0% **K** = 10% * Coating standard	**B** = ± 25ppm/°C **D** = ± 50ppm/°C **E** = ± 100ppm/°C	**G** = Gold **S** = Solder

NOTE: Factory will convert order number into final part number

Vishay Electro-Films

Thin Film 0303 Size Resistor on Alumina



Product may not be to scale

FEATURES

- Chip size: 0.030 inches square
- Resistance range: 25Ω to 38kΩ
- Alumina substrate
- Low stray capacitance: < 0.2pF
- Resistor material: nichrome
- Resistor passivation coat optional
- Tolerances to 0.05%

The CC2 series single-value resistor chips offer a relatively small size, low shunt capacitance and solder pad option. The CC2s nichrome resistor material offers excellent stability. The CC2s are manufactured using Vishay Electro Films (EFI) sophisticated thin film equipment and manufacturing technology. The CC2s are 100% electrically tested and visually inspected to MIL-STD-883.

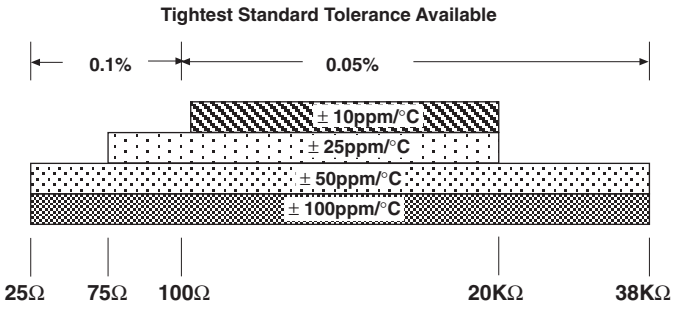
APPLICATIONS

Vishay EFI CC2 chip resistors provide excellent high-frequency response and are ideally suited for prototyping. Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

Recommended for hermetic environments where die is not exposed to moisture.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Moisture resistance, MIL-STD-202 Method 106 - Hermetic applications	± 0.2% maximum ΔR/R
Stability, 1000 hours, + 125°C, 100mW	± 0.1% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.1% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	100V
DC power rating at + 125°C (derated to zero at + 150°C)	100mW maximum
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

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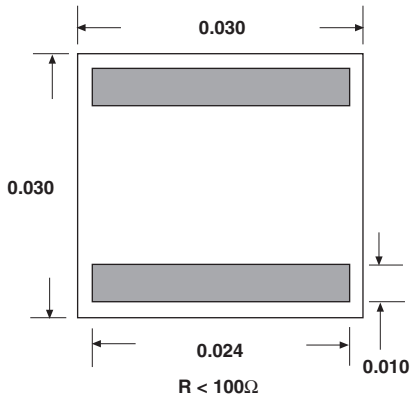
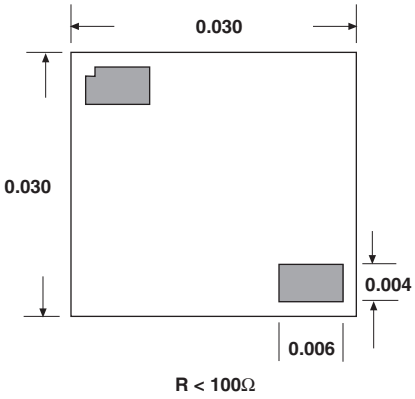
DIMENSIONS in inches





SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.030 x 0.030 ± 0.003 (1.27 x 1.27 ± 0.076mm)
Chip thickness	0.010 ± 0.002 (0.25 ± 0.05mm)
Chip substrate material	99.6% alumina, 2-4 µinch finish
Resistor material	Nichrome
Bonding pad size	0.004 x 0.006 (0.100 x 0.15mm) minimum
Number of pads	2
Pad material	25kÅ minimum gold standard
Backing	None

OPTIONS: Terminations: Aluminum, Nickel solder
Gold back for solder die attach
Contact Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 50Ω, ± 10%, ± 50ppm/°C TCR, Gold Terminations

W	CC2	5000	B	K	D	G
INSPECTION /PACKAGING	PRODUCT FAMILY	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE	TCR	TERMINATIONS
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)		Use first 4 significant digits of resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100	**A** = 0.05%* **B** = 0.1%* **C** = 0.25%* **D** = 0.5% **F** = 1.0% **G** = 2.0% **J** = 5.0% **K** = 10% *Coating standard	**A** = ± 10ppm/°C **B** = ± 25ppm/°C **D** = ± 50ppm/°C **E** = ± 100ppm/°C	**G** = Gold **S** = Solder

NOTE: Factory will convert order number into final part number

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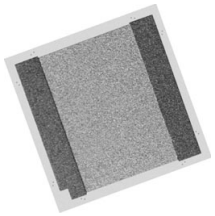
Vishay Electro-Films

Thin Film 0505 Size Resistor on Alumina



Product may not be to scale

FEATURES

- Chip size: 0.050 inches square
- Resistance range: 30Ω to 125kΩ
- Alumina substrate
- Low stray capacitance: < 0.2pF
- Resistor material: nichrome
- Resistor passivation coat optional
- Tolerances to 0.05%
- Solder pad optional

The CC3 series single-value resistor chips offer a relatively small size, low shunt capacitance and solder pad option. The CC3s nichrome resistor material offers excellent stability. The CC3s are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CC3s are 100% electrically tested and visually inspected to MIL-STD-883.

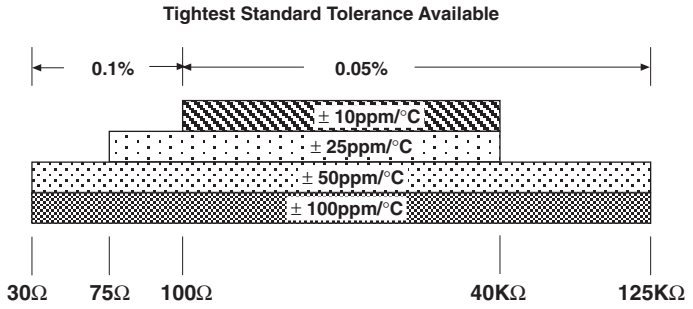
APPLICATIONS

Vishay EFI CC3 chip resistors provide excellent high-frequency response and are ideally suited for prototyping. Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

Recommended for hermetic environments where die is not exposed to moisture.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Moisture resistance, MIL-STD-202 Method 106 - Hermetic applications	± 0.2% maximum ΔR/R
Stability, 1000 hours, + 125°C, 100mW	± 0.1% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.1% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	100V
DC power rating at + 125°C (derated to zero at + 150°C)	100mW maximum
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

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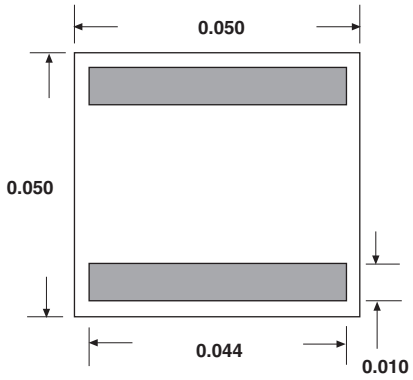
DIMENSIONS in inches



SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.050 x 0.050 ± 0.003 (1.27 x 1.27 ± 0.076mm)
Chip thickness	0.010 ± 0.002 (0.25 ± 0.05mm)
Chip substrate material	99.6% alumina, 2-4 µinch finish
Resistor material	Nichrome
Bonding pad size	0.010 x 0.044 (0.254 x 0.117mm) minimum
Number of pads	2
Pad material	25kÅ minimum gold standard
Backing	None

OPTIONS: Terminations: Aluminum, Nickel solder (62/32)
Gold back for solder die attach
Contact Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 50Ω, ± 10%, ± 50ppm/°C TCR, Gold Terminations

W	**CC3**	**5000**	**B**	**K**	**D**	**G**
INSPECTION /PACKAGING	PRODUCT FAMILY	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE	TCR	TERMINATIONS
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)		Use first 4 significant digits of resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100	**A** = 0.05%* **B** = 0.1%* **C** = 0.25%* **D** = 0.5% **F** = 1.0% **G** = 2.0% **J** = 5.0% **K** = 10% *Coating standard	**A** = ± 10ppm/°C **B** = ± 25ppm/°C **D** = ± 50ppm/°C **E** = ± 100ppm/°C	**G** = Gold **S** = Solder

Vishay Electro-Films

Thin Film 0510 Size Resistor on Alumina

Product may not be to scale

FEATURES

- Chip size: 0.050 x 0.100 inches
- Resistance range: 50Ω to 400kΩ
- Alumina substrate
- Low stray capacitance: < 0.2pF
- Resistor material: nichrome
- Resistor passivation coat optional
- Tolerances to 0.05%
- Solder pad optional

The CC4 series single-value resistor chips offer increased power in larger size, low shunt capacitance and solder pad option. The CC4s nichrome resistor material offers excellent stability.

The CC4s are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CC4s are 100% electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

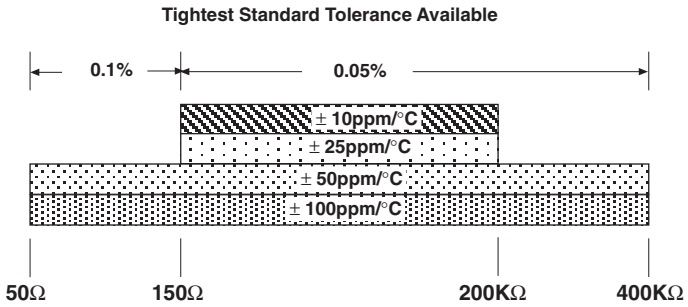
Vishay EFI CC4 chip resistors provide excellent high-frequency response and are ideally suited for prototyping.

Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

Recommended for hermetic environments where die is not exposed to moisture.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Moisture resistance, MIL-STD-202 Method 106 - Hermetic applications	± 0.2% maximum ΔR/R
Stability, 1000 hours, + 125°C, 175mW	± 0.1% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.1% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 125°C (derated to zero at + 150°C)	175mW maximum
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

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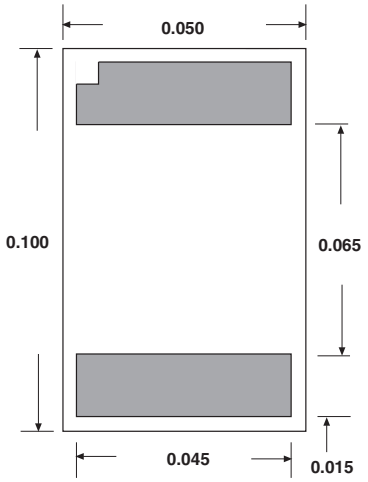
DIMENSIONS in inches



SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.050 x 0.100 ± 0.003 (1.27 x 2.54 ± 0.076mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	99.6% alumina, 2-4 µinch finish
Resistor material	Nichrome
Bonding pad size	0.015 x 0.045 (0.381 x 1.143mm) minimum
Number of pads	2
Pad material	25kÅ minimum gold standard
Backing	None

OPTIONS: Terminations: Aluminum, Nickel solder (62/32)
Gold back for solder die attach
Contact Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 80Ω, ± 10%, ± 50ppm/°C TCR, Gold Terminations

W	**CC4**	**8000**	**B**	**K**	**D**	**G**
INSPECTION /PACKAGING	PRODUCT FAMILY	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE	TCR	TERMINATIONS
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)		Use first 4 significant digits of resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100	**A** = 0.05%* **B** = 0.1%* **C** = 0.25%* **D** = 0.5% **F** = 1.0% **G** = 2.0% **J** = 5.0% **K** = 10% *Coating standard	**A** = ± 10ppm/°C **B** = ± 25ppm/°C **D** = ± 50ppm/°C **E** = ± 100ppm/°C	**G** = Gold **S** = Solder

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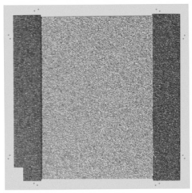
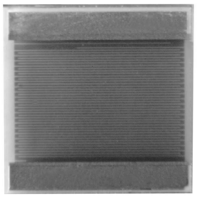
Thin Film 1010 Size Resistor on Alumina





Product may not be to scale

The CC5 series single-value resistor chips offer increased power in larger size, low shunt capacitance and solder pad option. The CC5s nichrome resistor material offers excellent stability.

The CC5s are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CC5s are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- Chip size: 0.100 inches square
- Resistance range: 50Ω to 1MΩ
- Alumina substrate
- Low stray capacitance: < 0.2pF
- Resistor material: nichrome
- DC power rating: 400mW
- Resistor passivation coat optional
- Tolerances to 0.05%
- Solder pad optional

APPLICATIONS

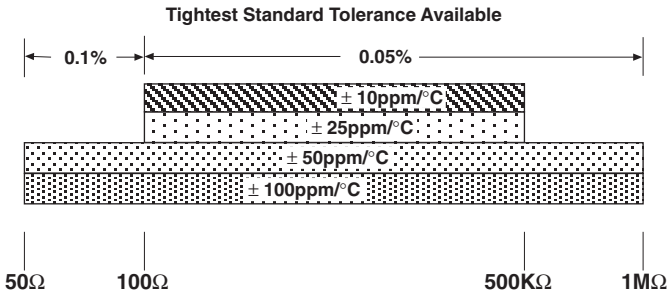
Vishay EFI CC5 chip resistors have excellent power dissipation capability and are ideally suited for prototyping. Not suitable for high moisture applications unless protected.

Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

Recommended for hermetic environments where die is not exposed to moisture.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Stability, 1000 hours, + 125°C	± 0.1% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.25% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	200V maximum
DC power rating at + 125°C (derated to zero at + 150°C)	400mW maximum
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

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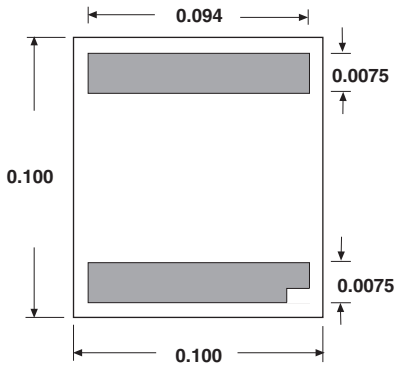
DIMENSIONS in inches



SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.100 x 0.100 ± 0.003 (2.54 x 2.54 ± 0.076mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	99.6% alumina
Resistor material	Nichrome
Bonding pad size	0.0075 x 0.094 (0.190 x 2.375mm) minimum
Number of pads	2
Pad material	25kÅ minimum gold standard
Backing	None

OPTIONS: Terminations: Aluminum, Nickel solder (62/32)
Gold back for solder die attach
Contact Applications Engineer

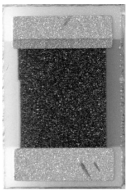
ORDERING INFORMATION

Example: 100% visual, 80Ω, ± 10%, ± 50ppm/°C TCR, Gold Terminations

W	**CC5**	**8000**	**B**	**K**	**D**	**G**
INSPECTION /PACKAGING	PRODUCT FAMILY	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE	TCR	TERMINATIONS
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)		Use first 4 significant digits of resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100	**A** = 0.05%* **B** = 0.1%* **C** = 0.25%* **D** = 0.5% **F** = 1.0% **G** = 2.0% **J** = 5.0% **K** = 10% *Coating standard	**A** = ± 10ppm/°C **B** = ± 25ppm/°C **D** = ± 50ppm/°C **E** = ± 100ppm/°C	**G** = Gold **S** = Solder

Vishay Electro-Films

Thin Film 0304 Size Resistor on Alumina



Product may not be to scale

FEATURES

- Chip size: 0.030 x 0.045 inches
- Resistance range: 20Ω to 59kΩ
- Alumina substrate
- Low stray capacitance: < 0.2pF
- Resistor material: nichrome
- Resistor passivation coat optional
- Tolerances to 0.05%
- Solder pad optional

The CC6 series single-value resistor chips offer a small size, low shunt capacitance and solder pad option.
The CC6s nichrome resistor material offers excellent stability.
The CC6s are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CC6s are 100% electrically tested and visually inspected to MIL-STD-883.

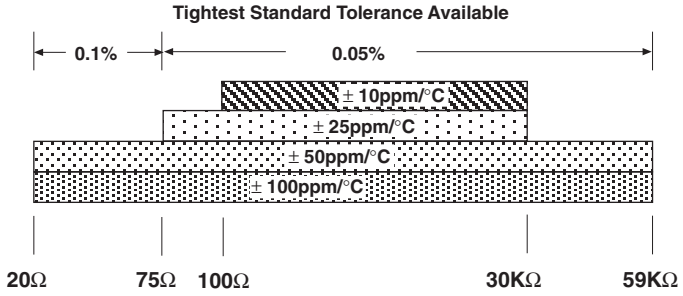
APPLICATIONS

Vishay EFI CC6 chip resistors provide excellent high-frequency response and are ideally suited for prototyping.
Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

Recommended for hermetic applications where die is not exposed to moisture.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Moisture resistance, MIL-STD-202 Method 106 - Hermetic applications	± 0.2% maximum ΔR/R
Stability, 1000 hours, + 125°C, 65mW	± 0.1% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.1% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 125°C (derated to zero at + 150°C)	65mW maximum
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

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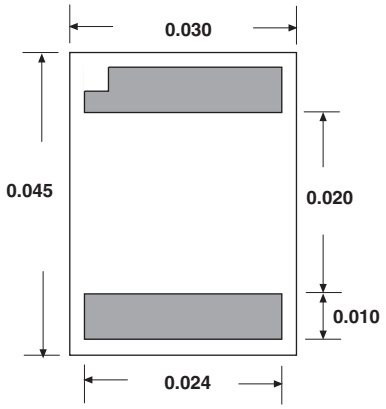
• SWEDEN +46.8.594.70590 FAX: +46.8.594.70581 • UK +44 191 514 8237 FAX: +44 1953 457 722 • USA: (401) 738-9150 FAX: (401) 738-4389

DIMENSIONS in inches



SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.030 x 0.045 ± 0.003 (0.762 x 1.143 ± 0.076mm)
Chip thickness	0.010 ± 0.002 (0.25 ± 0.05mm)
Chip substrate material	99.6% alumina, 2-4 microinch finish
Resistor material	Nichrome
Bonding pad size	0.010 x 0.024 (0.254 x 0.61mm) minimum
Number of pads	2
Pad material	25kÅ minimum gold standard
Backing	None

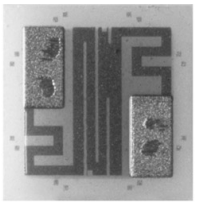
OPTIONS: Terminations: Aluminum, Nickel solder (62/32)
Gold back for solder die attach
Contact Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 50Ω, ± 10%, ± 50ppm/°C TCR, Gold Terminations

W	**CC6**	**5000**	**B**	**K**	**D**	**G**
INSPECTION /PACKAGING	PRODUCT FAMILY	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE	TCR	TERMINATIONS
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)		Use first 4 or 5 significant digits of resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100	**A** = 0.05%* **B** = 0.1%* **C** = 0.25%* **D** = 0.5% **F** = 1.0% **G** = 2.0% **J** = 5.0% **K** = 10% *Coating standard	**A** = ± 10ppm/°C **B** = ± 25ppm/°C **D** = ± 50ppm/°C **E** = ± 100ppm/°C	**G** = Gold **S** = Solder

Thin Film 0202 Size Resistor on Alumina



Product may not be to scale

The CC8 series resistor chips offer a combination of low shunt capacitance, small size and excellent stability.
The CC8s are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CC8s are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- Chip size: 0.020 inches square
- Resistance range: 20Ω to 20kΩ
- Alumina substrate
- Low stray capacitance: < 0.2pF
- Resistor material: nichrome with passivation coat
- Tolerances to 0.5%

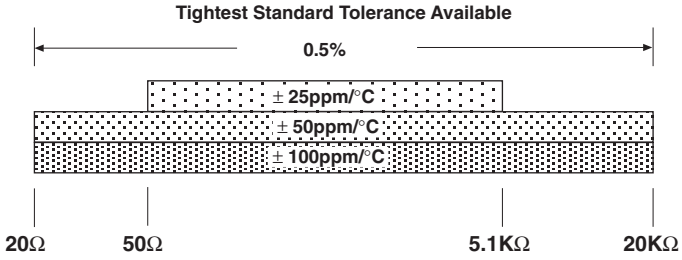
APPLICATIONS

Vishay EFI CC8 chip resistors provide excellent high-frequency response and are ideally suited for prototyping.
Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

Recommended for hermetic environment where die is not exposed to moisture.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
303	308
302	307
301	306

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Moisture resistance, MIL-STD-202 Method 106 (Passivated film)	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 25mW	± 0.2% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 1000 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at + 150°C)	35mW maximum
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

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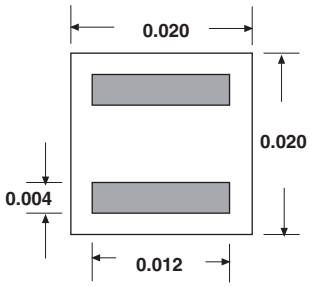
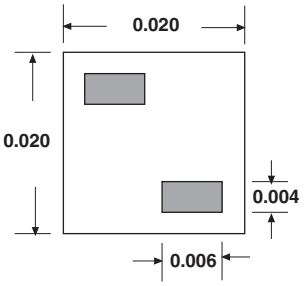
• SWEDEN +46.8.594.70590 FAX: +46.8.594.70581 • UK +44 191 514 8237 FAX: +44 1953 457 722 • USA: (401) 738-9150 FAX: (401) 738-4389

DIMENSIONS in inches



TYPICAL RANGE
20Ω - 49Ω



TYPICAL RANGE
50Ω - 20KΩ

SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.020 x 0.020 ± 0.003 (0.5 x 0.5 ± 0.08mm)
Chip thickness	0.010 ± 0.002 (0.25 ± 0.05mm)
Chip substrate material	99.6% alumina, 2-4 microinch finish
Resistor material	Nichrome
Bonding pad size	0.004 x 0.006 (0.10 x 0.15mm) minimum
Number of pads	2
Pad material	25kÅ minimum gold standard
Passivation	Thermalset Plastic
Backing	None

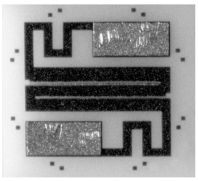
OPTIONS: Gold back for solder die attach
Contact Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 50Ω, ± 10%, ± 50ppm/°C TCR, Gold Pads, Class H Visual inspection

W	**CC8**	**302**	**5000**	**B**	**K**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use first 4 significant digits of resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10	**D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Thin Film 0202 Size Resistor on Alumina



Product may not be to scale

The SFC series resistor chips offer a combination of low shunt capacitance and small size. The SFCs tantalum nitride resistor material offers excellent resistance to high moisture environments.
The SFCs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology.
The SFCs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

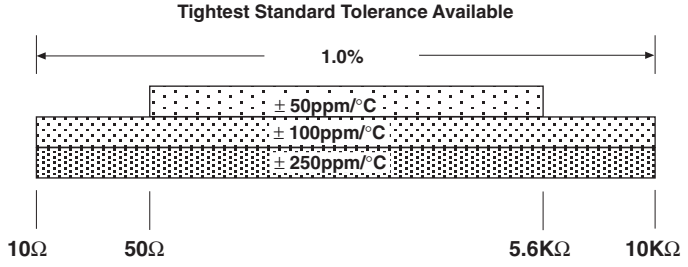
- Small size: 0.020 inches square
- Resistance range: 10Ω to 10KΩ
- Alumina substrate
- Low shunt capacitance: < 0.2pF
- Resistor material: tantalum nitride
- Moisture resistant

APPLICATIONS

Vishay EFI SFC chip resistors provide excellent high-frequency response and are ideally suited for prototyping.
Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



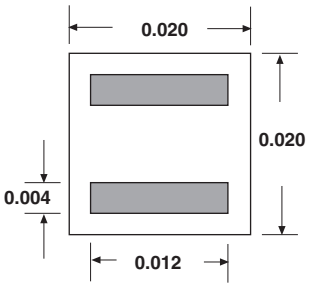
PROCESS CODE	
CLASS H*	CLASS K*
002	122
001	121
000	120

*MIL-PRF-38534 inspection criteria

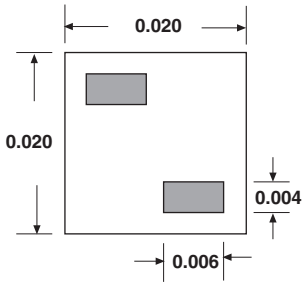
STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Moisture resistance, MIL-STD-202 Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 25mW	± 0.5% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at + 150°C)	62mW maximum
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

DIMENSIONS in inches



TYPICAL RANGE
10Ω - 49Ω



TYPICAL RANGE
50Ω - 10KΩ

SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.020 x 0.020 ± 0.003 (0.5 x 0.5 ± 0.768mm)
Chip thickness	0.010 ± 0.002 (0.25 ± 0.05mm)
Chip substrate material	99.6% alumina, 2-4 microinch finish
Resistor material	Tantalum nitride, self-passivating
Bonding pad size	0.004 x 0.006 (0.10 x 0.15mm) minimum
Number of pads	2
Pad material	25kÅ minimum gold standard
Backing	None

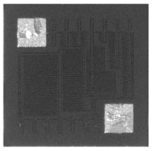
OPTIONS: Gold back for solder die attach
Contact Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 50Ω, ± 10%, ± 250ppm/°C TCR, Gold Pads, Class H Visual inspection

W	**SFC**	**000**	**5000**	**B**	**K**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use first 4 significant digits of resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10	**F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Thin Film Top-Contact Resistor



Product may not be to scale

The SFM series single-value resistor chips offer a small size, wide ohmic value range and excellent power capacity.
The SFMs tantalum nitride resistor material offers excellent resistance to high moisture environments.
The SFMs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The SFMs are 100% electrically tested and visually inspected to MIL-STD-883.

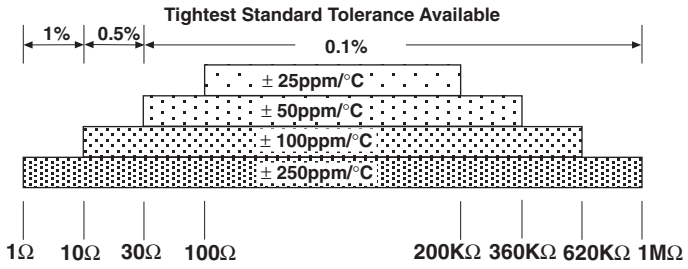
FEATURES

- Small size: 0.020 inches square
- Resistance range: 1.0Ω to 1MΩ
- DC power rating: 250mW
- Oxidized silicon substrate for good power dissipation
- Resistor material tantalum nitride, self passivating
- Moisture resistant

APPLICATIONS

Vishay EFI SFM top-contact resistor chips are designed to handle substantial power loads in many types of hybrid packages. They are ideally suited for this purpose because of their small size.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



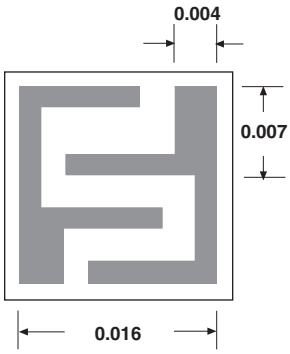
PROCESS CODE	
CLASS H*	CLASS K*
050	123
051	122
045	121
040	120

*MIL-PRF-38534 inspection criteria

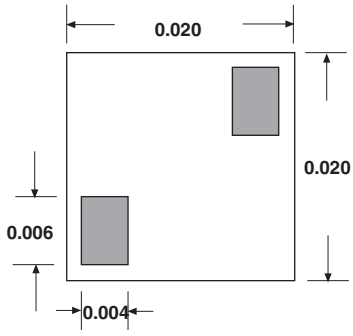
STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308 100Ω - 250kΩ < 100Ω or > 251kΩ	 - 35dB typical - 20dB typical
Moisture resistance, MIL-STD-202 Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 125mW	± 0.25% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at + 175°C)	250mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

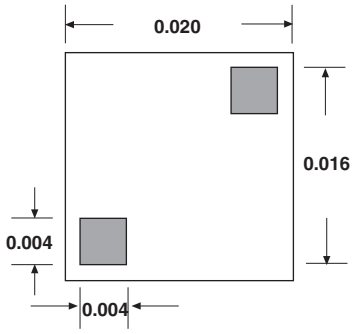
CONFIGURATIONS in inches



TYPICAL RANGE
1Ω - 29Ω



TYPICAL RANGE
30Ω - 819Ω



TYPICAL RANGE
820Ω - 1MΩ

SCHEMATIC

MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip size	0.020 x 0.020 ± 0.003 (0.5 x 0.5 ± 0.076mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pad size	0.004 x 0.004 (0.10 x 0.10mm)
Number of pads	2
Pad material	25kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

OPTIONS: Gold backing for eutectic die attach
Gold bonding pads, 15kÅ minimum thickness
Consult Applications Engineer

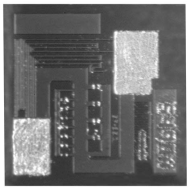
ORDERING INFORMATION

Example: 100% visual, 10KΩ, ± 1%, ± 100ppm/°C TCR, Aluminum Pads, Class H Visual inspection

W	**SFM**	**045**	**1000**	**1**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample , commercial visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use first 4 digits of resistance	**D** = 0.0001 **C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000 **4** = 10000	**B** = 0.1% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Vishay Electro-Films

Thin Film Top-Contact Resistor with Part Mark



Product may not be to scale

The SFP series single-value resistor chips offer a small size, wide ohmic value range and excellent power capacity.
The SFPs are part marked with resistance value allowing user the ability to visually determine the resistance value of the chip.
The SFPs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology.
The SFPs are 100% electrically tested and visually inspected to MIL-STD-883.

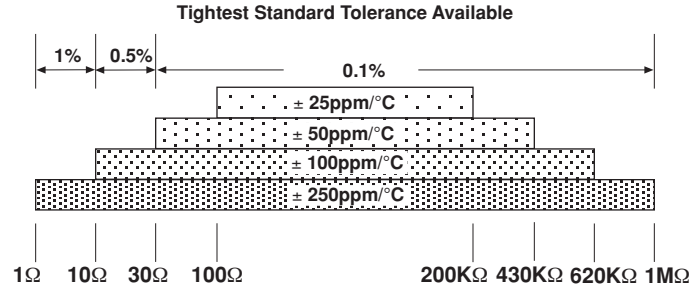
FEATURES

- Part marked - 5 digits
- Small size: 0.022 inches square
- Resistance range: 1Ω to 1MΩ
- DC power rating: 250mW
- Oxidized silicon substrate for good power dissipation
- Resistor material: tantalum nitride, self passivating
- Moisture resistant

APPLICATIONS

Vishay EFI SFP small resistor chips are widely used in hybrid packages where space is limited and chip value marking is important for identification. The die is part marked with the resistance value. Wire bonding is made to the two pads on the top of the chip.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
103	108
102	107
101	106
100	105

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308 100Ω - 250kΩ < 100Ω or > 251kΩ	 - 35dB typical - 20dB typical
Moisture resistance, MIL-STD-202 Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 125mW	± 0.25% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at + 175°C)	250mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

Values above 1M available

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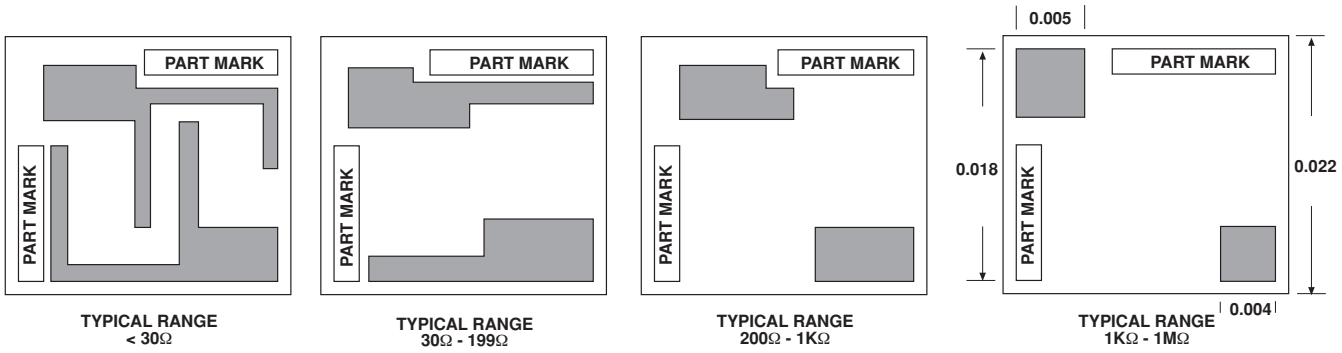
• SWEDEN +46.8.594.70590 FAX: +46.8.594.70581 • UK +44 191 514 8237 FAX: +44 1953 457 722 • USA: (401) 738-9150 FAX: (401) 738-4389

DIMENSIONS in inches



TYPICAL RANGE < 30Ω

TYPICAL RANGE 30Ω - 199Ω

TYPICAL RANGE 200Ω - 1KΩ

TYPICAL RANGE 1KΩ - 1MΩ

SCHEMATIC

STANDARD MARKING - 5 DIGITS

XXXX	**X**
Four significant digits of value	**Multiplier**
	C = 0.001
	B = 0.01
	A = 0.1
	0 = 0
	1 = 10
	2 = 100
	3 = 1000

MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip size	0.022 x 0.022 ± 0.003 (0.558 x 0.558 ± 0.05mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pad size	0.004 x 0.004 (0.10 x 0.10mm)
Number of pads	2
Pad material	25kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

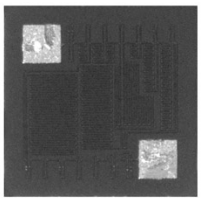
OPTIONS: Gold backing for eutectic die attach
Gold bonding pads, 15kÅ minimum thickness
Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 10KΩ, ± 1%, ± 250ppm/°C TCR, Aluminum Pads, Class H Visual inspection

W	**SFP**	**100**	**1000**	**1**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use first 4 digits of the resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000 **4** = 10000	**B** = 0.1% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

NiCr Thin Film, Top-Contact Resistor



Product may not be to scale

The SFN series resistor chips offer a combination of nichrome stability, good power rating and small size.
The SFNs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The SFNs are 100% electrically tested and visually inspected to MIL-STD-883.

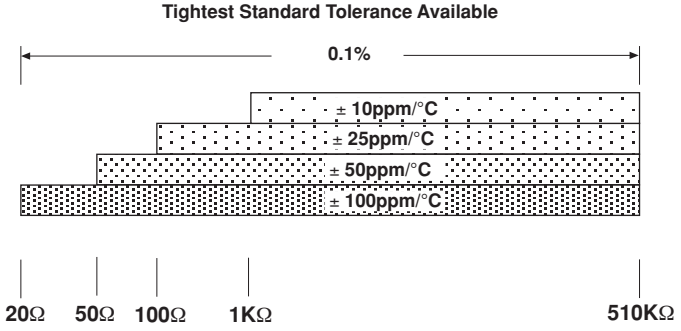
FEATURES

- Chip size: 20 inches square
- Resistance range: 10Ω to 510kΩ
- Resistor material: nichrome
- Oxidized silicon substrate
- 125mW power

APPLICATIONS

Vishay EFI SFN resistor chips are widely used in hybrid packages where space is limited. Designed with capacity to handle substantial power loads, they also have the benefit of nichrome stability.
Recommended for hermetic environments where die is not exposed to moisture.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



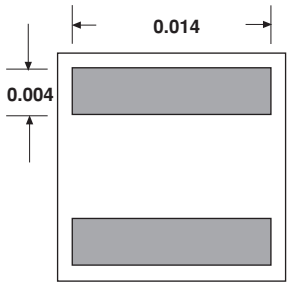
PROCESS CODE	
CLASS H*	CLASS K*
208	209
200	201
202	203
204	205

*MIL-PRF-38534 inspection criteria

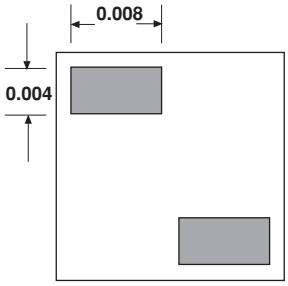
STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308 100Ω - 250kΩ < 100Ω or > 251kΩ	 - 35dB typical - 20dB typical
Stability, 1000 hours, + 125°C, 50mW	± 0.25% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at + 175°C)	125mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

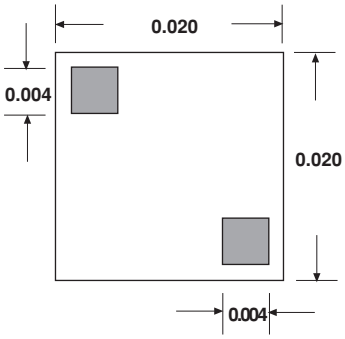
DIMENSIONS in inches



TYPICAL RANGE
10Ω - 55Ω



TYPICAL RANGE
56Ω - 7.4KΩ



TYPICAL RANGE
7.5KΩ - 510KΩ

SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.020 x 0.020 ± 0.003 (0.51 x 0.51 ± 0.05mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Nichrome (Passivation Optional)
Bonding pad size	0.004 x 0.004 (0.10 x 0.10mm)
Number of pads	2
Pad material	15kÅ minimum Gold
Backing	None, lapped semiconductor silicon

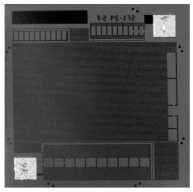
OPTIONS: Aluminum Pads
Passivation (thermal set plastic)
Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 10KΩ, ± 1%, ± 50ppm/°C TCR, Gold Pads, Class H Visual inspection

W	**SFN**	**202**	**1000**	**1**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use the first 4 significant digits of the resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000 **4** = 10000	**B** = 0.1% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Thin Film, Top-Contact Megohm Resistor



Product may not be to scale

The SFX series resistor chips extends the range of available resistance to 20 Meg. These offer one of the best combinations of small size and high value available.
The SFXs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The SFXs are 100% electrically tested and visually inspected to MIL-STD-883.

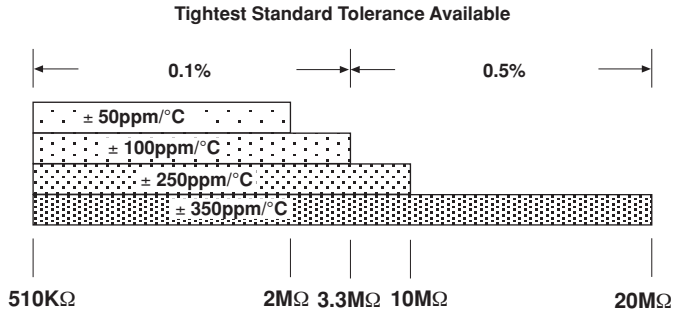
FEATURES

- Megohm resistance range: 0.51M to 20MΩ
- Chip size: 0.040 inches square
- Reduced hybrid size
- Resistor material: tantalum nitride, self-passivating
- Oxidized silicon substrate

APPLICATIONS

The SFX series megohm resistor chips are designed for use in hybrid packages which require small-size high-value resistors.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
059	155
054	156
017	158
018	157

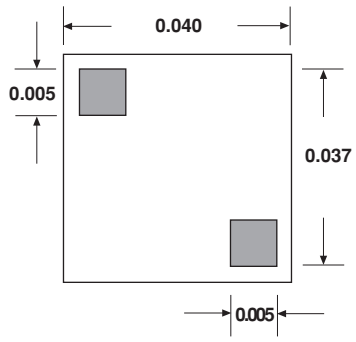
*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308	- 12dB typical
Moisture resistance, MIL-STD-202 Method 106, (Passivated only)	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 10mW	± 1.0% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at + 175°C)	20mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

VISHAY ELECTRO-FILMS • FRANCE +33.4.93.37.28.24 FAX: +33.4.93.37.27.31 • GERMANY +49.9287.710 FAX: +49 9287.70435 • ISRAEL +972.3.557.0945 FAX: +972.3.558.9121
• ITALY + 39.2.300.11911 FAX: +39.2.300.11999 • JAPAN +81.3.5464.6411 FAX: +81.3.5464.6433 • SINGAPORE +65.788.6668 FAX: +65.788.0988
• SWEDEN +46.8.594.70590 FAX: +46.8.594.70581 • UK +44 191 514 8237 FAX: +44 1953 457 722 • USA: (401) 738-9150 FAX: (401) 738-4389

DIMENSIONS in inches



SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.040 x 0.040 ± 0.003 (1.0 x 1.0 ± 0.075mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.050mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pad size	0.005 x 0.005 (0.127 x 0.127mm)
Number of pads	2
Pad material	10kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

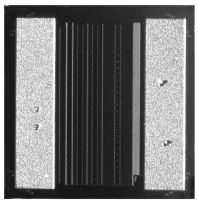
OPTIONS: Gold backing for eutectic die attach
Resistance values above 20M are available in 0.055 inches square size
0.030 inch square size also available with different values and TCR restrictions.
Consult Applications Engineer

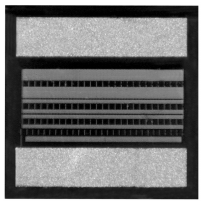
ORDERING INFORMATION

Example: 100% visual, 5MΩ, ± 1%, ± 250ppm/°C TCR, Aluminum Pads, Class H Visual inspection

W	**SFX**	**017**	**5000**	**3**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts, per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use the first 4 significant digits of the resistance	**2** = 100 **3** = 1000 **4** = 10000	**B** = 0.1% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10% **M** = 20% **L** = 25%

NiCr Thin Film, Top-Contact Resistor





Product may not be to scale

The SC3 series resistor chips on silicon offer a combination of nichrome stability, wide resistance range and higher power rating than is available on the same sized ceramic substrate.

The SC3's are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The SC3s are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- Small single chip size: 0.050 inches square
- Resistance range: 100Ω to 50kΩ
- Resistor material: nichrome
- Oxidized silicon substrate for good power dissipation
- 400mW capability
- User trimmable

APPLICATIONS

Vishay EFI SC3 chip resistors have excellent power dissipation capability and are ideally suited for prototyping.

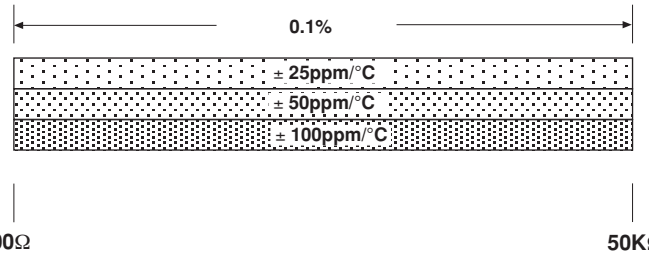
Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

Recommended for hermetic environments where die is not exposed to moisture.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES

Tightest Standard Tolerance Available



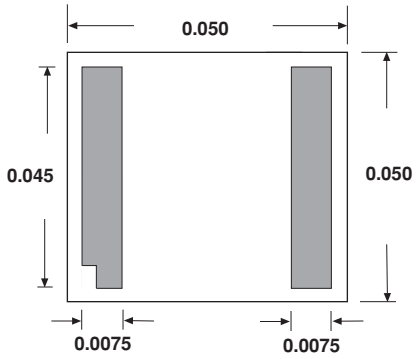
PROCESS CODE	
CLASS H*	CLASS K*
202	206
200	204
201	205

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Stability, 1000 hours, + 125°C	± 0.1% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.25% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at + 150°C)	400mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

DIMENSIONS in inches



SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.050 x 0.050 ± 0.003 (1.27 x 1.27 ± 0.076mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Nichrome
Bonding pad size	0.0075 x 0.045 (0.190 x 1.143mm) minimum
Number of pads	2
Pad material	15kÅ minimum gold standard
Backing	None, lapped semiconductor silicon

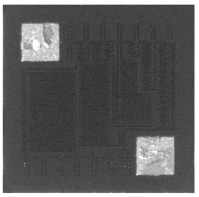
OPTIONS: Gold backing for eutectic die attach
Aluminum bonding pads, 10kÅ minimum thickness
User trimmable
Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 500Ω, ± 10%, ± 50ppm/°C TCR, Gold Pads, Class H Visual inspection

W	**SC3**	**200**	**5000**	**A**	**K**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use the first 4 significant digits of the resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100	**B** = 0.1% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Thin Film, Top-Contact Resistor



Product may not be to scale

The QFM series tantulum nitride on quartz single-value resistor chips offer a small size, wide ohmic value range and excellent frequency response.
The QFMs tantalum nitride resistor material offers excellent resistance to high moisture environments.
The QFMs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The QFMs are 100% electrically tested and visually inspected to MIL-STD-883.

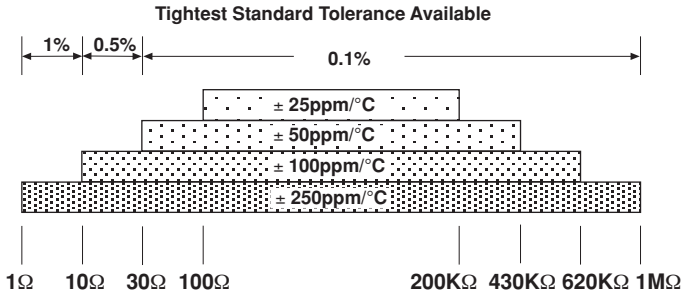
FEATURES

- Small size, 0.020 inches square
- Resistance range: 1.0Ω to 1MΩ
- DC power rating: 25mW
- Quartz substrate: < 0.1pF shunt capacitance
- Resistor material: tantalum nitride, self passivating
- Moisture resistant

APPLICATIONS

The QFM top-contact resistor chips are designed to handle substantial power loads in many types of hybrid packages. They are ideally suited for this purpose because of their small size.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



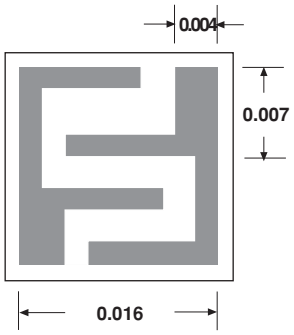
PROCESS CODE	
CLASS H*	CLASS K*
103	107
101	105
102	106
100	104
Aluminum Terminations	

*MIL-PRF-38534 inspection criteria

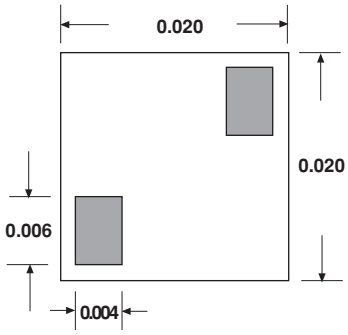
STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308 100Ω - 250kΩ < 100Ω or > 251kΩ	 - 35dB typical - 20dB typical
Moisture resistance, MIL-STD-202, Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 125mW	± (0.25% + 0.01Ω) maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at + 175°C)	25mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

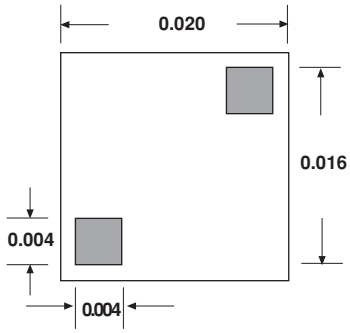
CONFIGURATIONS in inches



TYPICAL RANGE
1Ω - 29Ω



TYPICAL RANGE
30Ω - 819Ω



TYPICAL RANGE
820Ω - 1MΩ

SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.020 x 0.020 ± 0.003 (0.5 x 0.5 ± 0.076mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Quartz
Resistor material	Tantalum nitride, self-passivating
Bonding pad size	0.004 x 0.004 (0.10 x 0.10mm) minimum
Number of pads	2
Pad material	10kÅ minimum aluminum
Backing	None, lapped Quartz

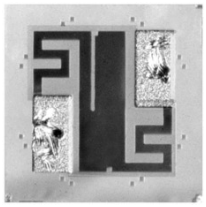
OPTIONS: Gold backing for eutectic die attach
Gold bonding pads, 15kÅ minimum thickness
Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 10KΩ, ± 1%, ± 100ppm/°C TCR, Aluminum Pads, Class H Visual inspection

W	**QFM**	**102**	**1000**	**1**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use the first 4 digits of the resistance	**D** = 0.0001 **C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000 **4** = 10000	**B** = 0.1% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

NiCr Thin Film, Top-Contact Resistor



Product may not be to scale

The QFN series nichrome on quartz resistor chips offer a combination of nichrome stability, excellent frequency response and small size.
The QFNs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The QFNs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

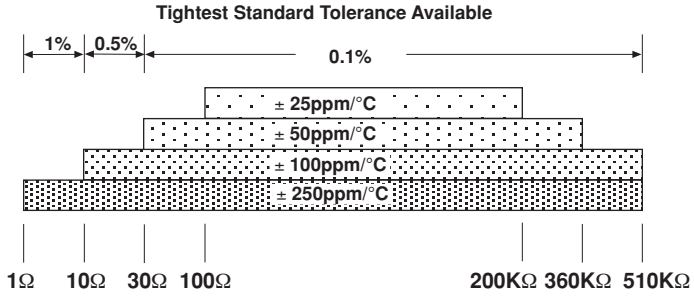
- Chip size: 0.020 inches square
- Resistance range: 10Ω to 510kΩ
- Resistor material: nichrome
- Quartz substrate: < 0.1pF shunt capacitance
- Power: 25mW

APPLICATIONS

Vishay EFI QFN top-contact resistor chips are widely used in hybrid packages where space is limited. Designed with capacity to handle substantial power loads, they also have the benefit of nichrome stability.

Recommended for hermetic environments where die is not exposed to moisture.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



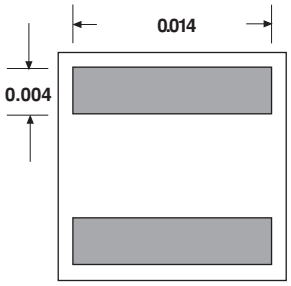
PROCESS CODE	
CLASS H*	CLASS K*
203	207
201	205
202	206
200	204
Gold Terminations	

*MIL-PRF-38534 inspection criteria

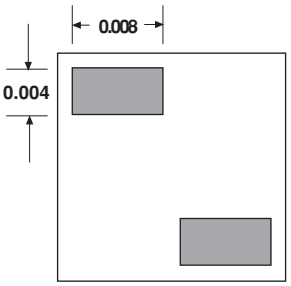
STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308 100Ω - 250kΩ < 100Ω or > 251kΩ	 - 35dB typical - 20dB typical
Stability, 1000 hours, + 125°C, 50mW	± 0.1% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at + 175°C)	25mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

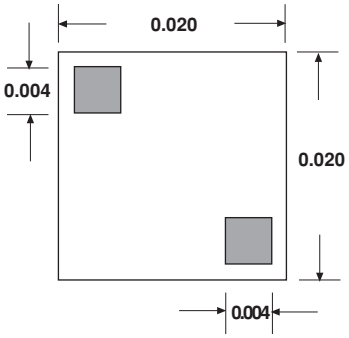
DIMENSIONS in inches



TYPICAL RANGE
10Ω - 55Ω



TYPICAL RANGE
56Ω - 7.4KΩ



TYPICAL RANGE
7.5KΩ - 510KΩ

SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.020 x 0.020 ± 0.003 (0.51 x 0.51 ± 0.05mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Quartz
Resistor material	Nichrome (Passivation Optional)
Bonding pad size	0.004 x 0.004 (0.10 x 0.10mm)
Number of pads	2
Pad material	15kÅ minimum gold
Backing	None, lapped Quartz

OPTIONS: Aluminum bonding pads, 10kÅ minimum thickness
Consult Applications Engineer

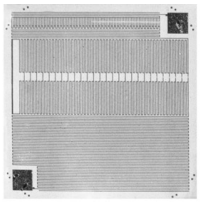
ORDERING INFORMATION

Example: 100% visual, 10KΩ, ± 1%, ± 50ppm/°C TCR, Gold Pads, Class H Visual inspection

W	**QFN**	**202**	**1000**	**1**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use the first 4 digits significant digits of the resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000 **4** = 10000	**B** = 0.1% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Available alternatives:
Aluminum pads or gold back
Passivation (thermal set plastic)

Thin Film, Top-Contact Megohm Resistor



Product may not be to scale

The QFX series, tantulum nitride on quartz resistor chips combine high resistance with low shunt capacitance. These offer one of the best combinations of small size, frequency response and high value available.
The QFXs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The QFXs are 100% electrically tested and visually inspected to MIL-STD-883.

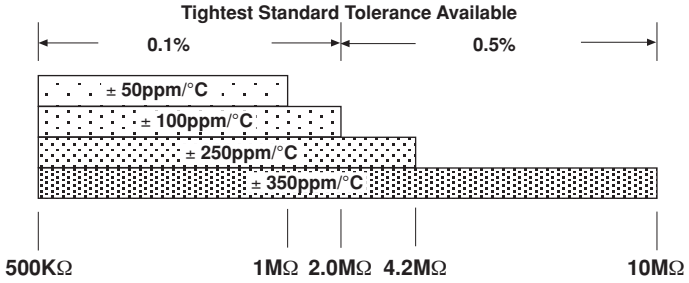
FEATURES

- Chip size: 0.050 inches square
- Resistance range: 500kΩ to 10MΩ
- Quartz substrate: < 0.1pF shunt capacitance
- Resistor material: tantalum nitride, self-passivating

APPLICATIONS

The QFX series resistor chips are designed for circuits requiring high values with lower shunt capacitance for higher frequency of operation.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
012	174
009	175
013	176
014	177

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308	- 12dB typical
Moisture resistance, MIL-STD-202 Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 10mW	± 0.5% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	400V maximum
DC power rating at + 70°C (derated to zero at + 175°C)	20mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

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• ITALY + 39.2.300.11911 FAX: +39.2.300.11999 • JAPAN +81.3.5464.6411 FAX: +81.3.5464.6433 • SINGAPORE +65.788.6668 FAX: +65.788.0988
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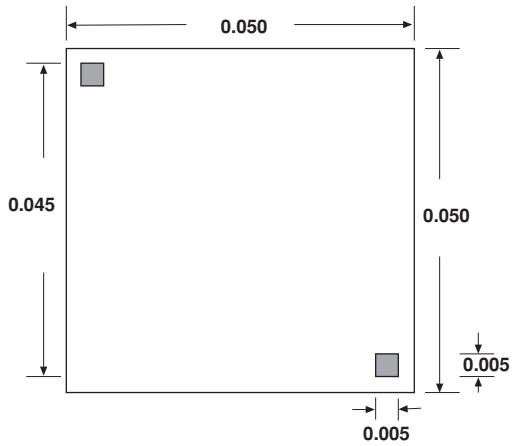
DIMENSIONS in inches



SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.050 x 0.050 ± 0.003 (1.25 x 1.25 ± 0.75mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Quartz
Resistor material	Tantalum nitride, self-passivating
Bonding pad size	0.005 x 0.005 (0.127 x 0.127mm)
Number of pads	2
Pad material	10kÅ minimum aluminum
Backing	None, lapped Quartz

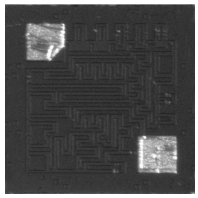
OPTIONS: Gold bonding pads, 15kÅ minimum
Consult Applications Engineer

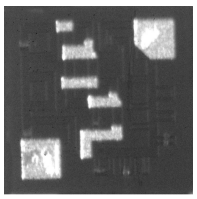
ORDERING INFORMATION

Example: 100% visual, 5MΩ, ± 1%, ± 350ppm/°C TCR, 50 mil, Aluminum Pads, Class H Visual inspection

W	**QFX**	**014**	**5000**	**3**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use the first 4 digits significant digits of the resistance	**1** = 10 **2** = 100 **3** = 1000 **4** = 10000	**B** = 0.1% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10% **M** = 20% **L** = 25%

Thin Film, Back-Contact Resistor





Product may not be to scale

The Back Contact Resistor (BCR) series single-value back-contact resistor chip is one of the smallest chips available. The BCR requires only one wire bond thus saving hybrid space. The BCRs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The BCRs are 100% electrically tested and visually inspected to MIL-STD-883.

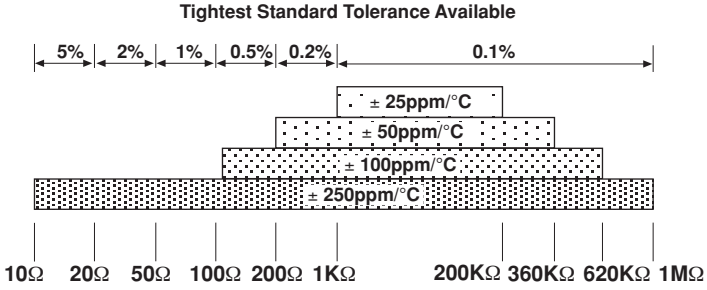
FEATURES

- Only one wire bond required
- Small size: 0.020 inches square.
- Resistance range: 10Ω to 1MΩ
- Oxidized silicon substrate for good power dissipation
- Resistor material: tantalum nitride, self-passivating
- Moisture resistant

APPLICATIONS

Vishay EFI BCR resistor chips are widely used in hybrid packages where space is limited. The bottom connection is made by attaching the back of the chip to the substrate either eutectically or with conductive epoxy. The single wire bond is made to the notched pad on the top of the chip. (The other rectangular pad on the top of the chip is a via hole, a low-ohmic contact connecting the resistor to the bottom of the chip.)

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
010	056
002	061
027	059
008	052

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308 100Ω - 250kΩ < 100Ω or > 251kΩ	 - 35dB typical - 20dB typical
Moisture resistance, MIL-STD-202 Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 125mW	± 1.0% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	75V maximum
DC power rating at + 70°C (derated to zero at + 175°C)	250mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

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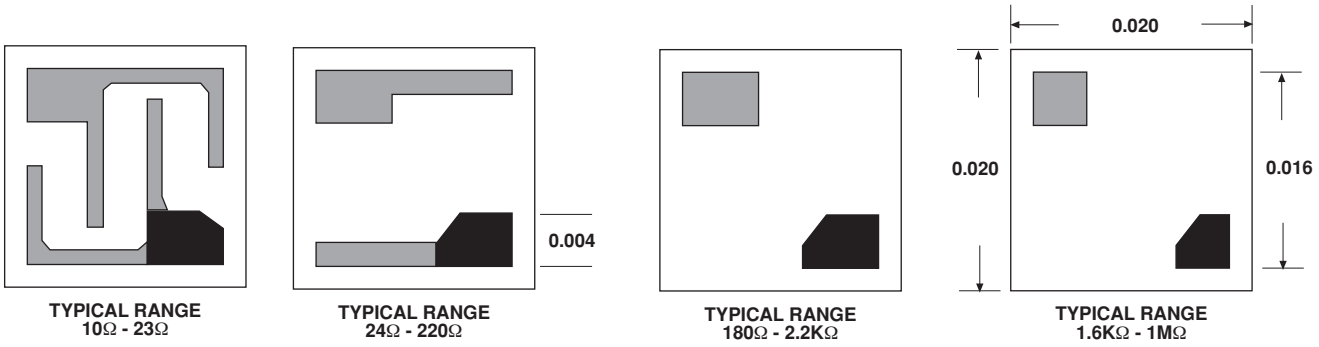
DIMENSIONS in inches



TYPICAL RANGE 10Ω - 23Ω

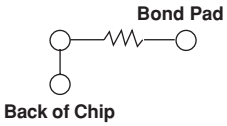
TYPICAL RANGE 24Ω - 220Ω

TYPICAL RANGE 180Ω - 2.2KΩ

TYPICAL RANGE 1.6KΩ - 1MΩ

NOTE: Notched shaded area represents top bonding pad. The backside of the chip constitutes the second resistor connection.

SCHEMATIC



MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.020 x 0.020 ± 0.002 (0.50 x 0.50 ± 0.05mm)
Chip thickness	0.010 ± 0.003 (0.253 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pad size	0.004 x 0.004 (0.100 x 0.100mm)
Number of pads	1
Pad material	10kÅ minimum aluminum
Backing	3kÅ minimum gold
Recommended attachment method	Eutectic or conductive epoxy

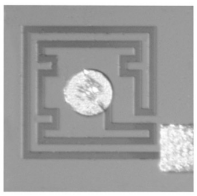
OPTIONS: Gold bonding pads, 15kÅ minimum thickness.
Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 16kΩ, ± 1%, ± 250ppm/°C TCR, Aluminum Pads, Class H Visual inspection

W	**BCR**	**008**	**1600**	**1**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use first 4 digits significant digits of the resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000	**B** = 0.1% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Miniature Back-Contact Resistor Chip

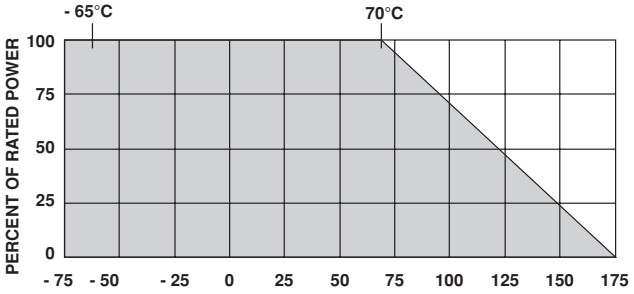


Product may not be to scale

The BCM series are the smallest single value chips available from Vishay EFI. One wire bond only, they are intended for loose tolerance commercial applications.
The BCMs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The BCMs are 100% electrically tested and visually inspected to Vishay EFI's commercial criteria.

FEATURES

- Only one wire bound required
- Small size: 0.015 inches square
- Single top contact
- Resistance range: 100Ω to 100kΩ (See Standard RETMA Chart)
- Tolerance: ± 10%, ± 20%, ± 25%, ± 50%
- Packaging: Matrix tray

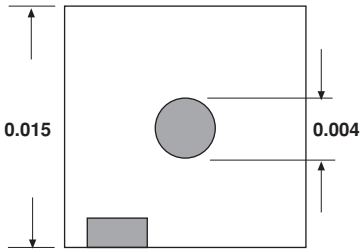


DERATING CURVE

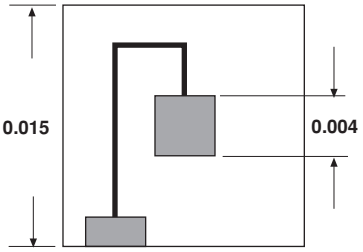
STANDARD VALUE RETMA CHART		
TOLERANCE		
± 10%		± 20%
10	33	10
12	39	15
15	47	22
18	56	33
22	68	47
27	82	68

STANDARD ELECTRICAL SPECIFICATIONS	
PARAMETER	
TCR	± 250ppm/°C
Noise, MIL-STD-202, Method 106	-20dB typical
Moisture resistance, MIL-STD-202 Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 50mW	± 1.0% maximum ΔR/R
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.5% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.25% maximum ΔR/R
Insulation resistance (open resistor)	10^{12} minimum
Operating voltage	100V maximum
Power rating at + 70°C (See Derating Curve)	100mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.5% maximum ΔR/R

CONFIGURATIONS in inches

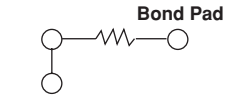


TYPICAL RANGE
821Ω - 100KΩ



TYPICAL RANGE
100Ω - 820Ω

SCHEMATIC



MECHANICAL SPECIFICATIONS in inches

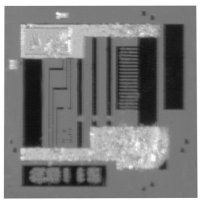
PARAMETER	
Chip size	0.015 x 0.015 ± 0.002 (0.381 x 0.381 ± 0.05mm)
Chip thickness	0.008 ± 0.003 (0.203 ± 0.08mm)
Chip substrate material	Silicon
Resistor material	Tantalum nitride, self-passivating
Bonding pad size	0.0038 square minimum - 0.004 square typical
Number of pads	1 top
Pad material	Aluminum 10kÅ thick
Backing	3kÅ minimum gold

ORDERING INFORMATION

Example: 100% visual, 100kΩ, ± 10%, ± 250ppm/°C TCR, Aluminum Pads, Commercial Inspection.

W	**BCM**	**000**	**1000**	**2**	**K**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use first 4 digits significant digits of the resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100	**K** = 10% **M** = 20% **L** = 25% **N** = 50%

Thin Film Back-Contact Resistor with Part Mark



Product may not be to scale

The BCP series single-value back-contact resistor chip requires only one wire bond, thus saving hybrid space.
The BCPs are part marked with resistance value allowing user the ability to visually determine the resistance value of the chip.
The BCPs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The BCPs are 100% electrically tested and visually inspected to MIL-STD-883.

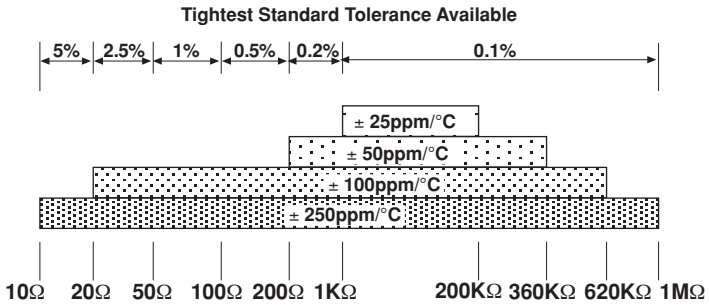
FEATURES

- Only one wire bond required
- Part marked - 5 digits maximum
- Smallest size: 0.022 inches square
- Resistance range: 10Ω to 1MΩ
- Oxidized silicon substrate for good power dissipation
- Resistor material: tantalum nitride, self-passivating
- Moisture resistant

APPLICATIONS

Vishay EFI BCP resistor chips are widely used in hybrid packages where space is limited. The bottom connection is made by attaching the back of the chip to the substrate either eutectically or with conductive epoxy. The single wire bond is made to the notched pad on the top of the chip. (The other rectangular pad on the top of the chip is a via hole, a low-ohmic contact connecting the resistor to the bottom of the chip.) The die is part marked with the resistance value.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
103	133
102	132
101	131
100	130

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308 100Ω - 250kΩ < 100Ω or > 251kΩ	 - 35dB typical - 20dB typical
Moisture resistance, MIL-STD-202 Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 125mW	± 1.0% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	100V
Insulation resistance	10^{12} minimum
Operating voltage	75V maximum
DC power rating at + 70°C (derated to zero at + 175°C)	250mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

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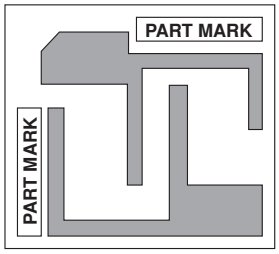
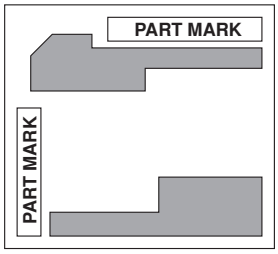
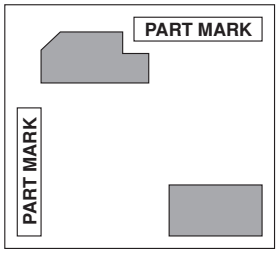
DIMENSIONS in inches



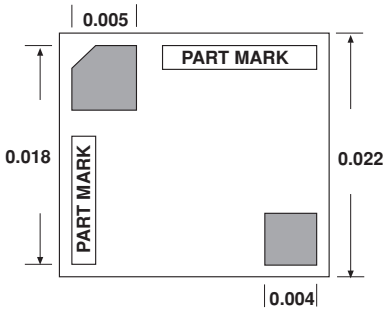
TYPICAL RANGE
< 30Ω



TYPICAL RANGE
30Ω - 199Ω



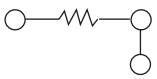
TYPICAL RANGE
200Ω - 1KΩ



TYPICAL RANGE
1KΩ - 1MΩ

STANDARD MARKING - 5 DIGITS	
XXXX **Four significant digits of value**	**X** **Multiplier** **C = 0.001** **B = 0.01** **A = 0.1** **0 = 0** **1 = 10** **1 = 100** **3 = 1000**

SCHEMATIC



BACK OF DIE

MECHANICAL SPECIFICATIONS in inches

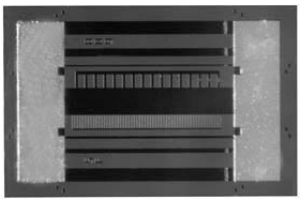
PARAMETER	
Chip size	0.022 x 0.022 ± 0.002 (0.55 x 0.55 ± 0.05mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pad size	0.005 x 0.005 (0.127 x 0.127mm)
Number of pads	1
Pad material	10kÅ minimum aluminum
Backing	3kÅ minimum gold
Recommended attachment method	Eutectic or conductive epoxy

ORDERING INFORMATION

Example: 100% visual, 10kΩ, ± 1%, ± 250ppm/°C TCR, Aluminum Pads, Class H Visual inspection

W	**BCP**	**100**	**1000**	**1**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use first 4 digits significant digits of the resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000 **4** = 10000	**B** = 0.1% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Thin Film Power Resistors



Product may not be to scale

The PWA series resistor chips offer a 500mW power rating in a small size. These offer one of the best combinations of size and power available.
The PWAs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The PWAs are 100% electrically tested and visually inspected to MIL-STD-883.

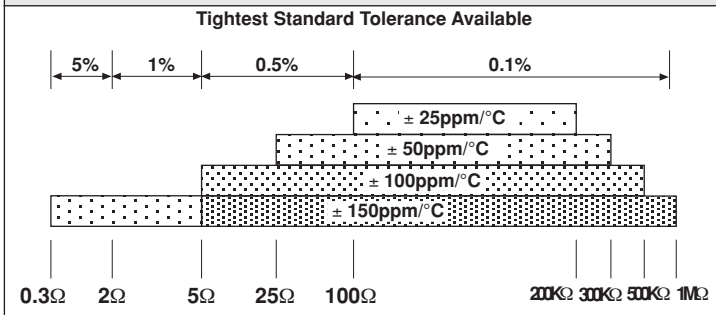
FEATURES

- 500mW power
- Chip size: 0.030 x 0.045 inches
- Resistance range 0.3Ω to 1MΩ
- Oxidized silicon substrate for good power dissipation
- Resistor material: Tantalum nitride, self-passivating

APPLICATIONS

The PWA resistor chips are used mainly in higher power circuits of amplifiers where increased power loads require a more specialized resistor.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



*600, - 100ppm R < 2Ω, ± 250ppm for 2Ω to 5Ω

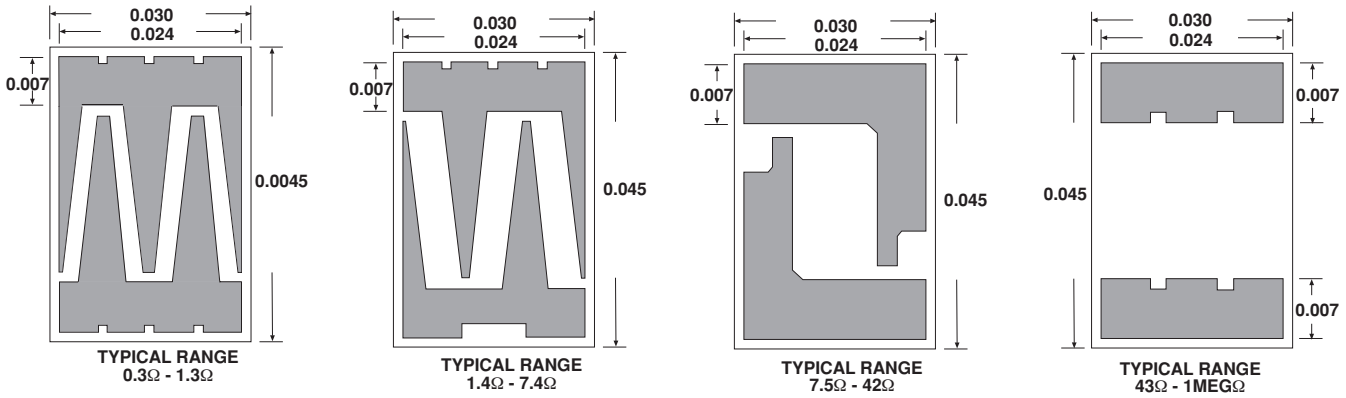
PROCESS CODE	
CLASS H*	CLASS K*
002	006
001	005
000	008
009	010

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308 100Ω - 250kΩ < 100Ω or > 251kΩ	 - 35dB typical - 20dB typical
Moisture resistance, MIL-STD-202 Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 250mW	± 0.5% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.1% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.2% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage steady state 5 x rated power	 100V maximum 200V maximum
DC power rating at + 70°C (derated to zero at + 175°C) (Conductive epoxy die attach to alumina substrate)	500mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.1% maximum ΔR/R

DIMENSIONS in inches



SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.030 x 0.045 ± 0.002 (0.762 x 1.143 ± 0.5mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pad size	0.007 x 0.024 (0.1778 x 0.6096mm)
Number of pads	2
Pad material	10kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

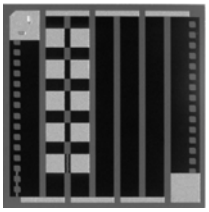
OPTIONS: Gold back for eutectic die attach
Gold bonding pads, 15kÅ minimum thickness
Contact Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 10kΩ, ± 1%, ± 100ppm/°C TCR, Aluminum Pads, Class H Visual inspection

W	**PWA**	**000**	**1000**	**1**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use first 4 digits significant digits of the resistance	**D** = 0.0001 **C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000	**B** = 0.1% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Thin Film Power Resistors



Product may not be to scale

FEATURES

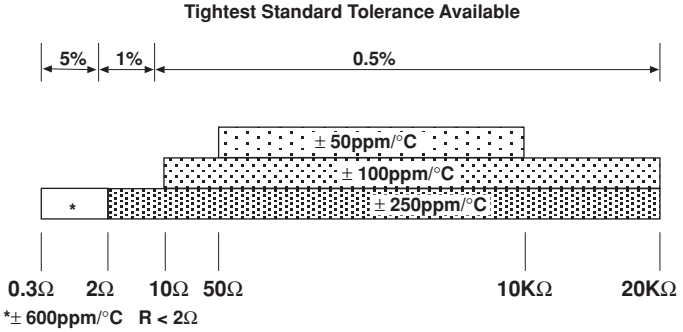
- Power: 1 watt
- Chip size: 0.070 inches square
- Resistance range: 0.3Ω to 20kΩ
- Oxidized silicon substrate for good power dissipation
- Resistor material: tantalum nitride, self-passivating

The PWB series resistor chips offer a 1 watt power rating in a relatively small size. They offer one of the best combinations of size and power available.
The PWBs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The PWBs are 100% electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

The PWB resistor chips are used mainly in higher power circuits of amplifiers where increased power loads require a more specialized resistor.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
001	005
000	004
008	009

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308 100Ω - 250kΩ < 100Ω or > 251kΩ	 - 35dB typical - 20dB typical
Moisture resistance, MIL-STD-202 Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 500mW	± 0.5% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.1% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.2% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage steady state 5 x rated power	 100V maximum 200V maximum
DC power rating at + 70°C (derated to zero at + 175°C) (Conductive epoxy die attach to alumina substrate)	1 Watt
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R%

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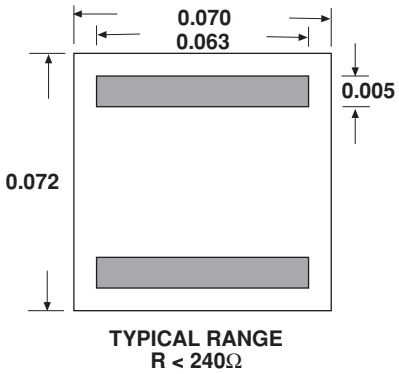
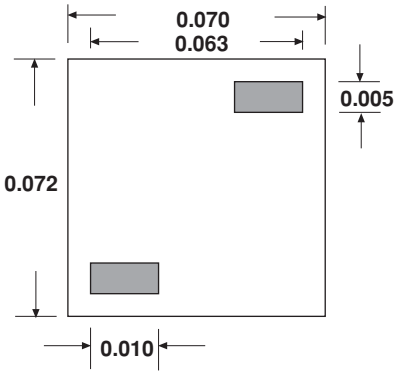
• ITALY + 39.2.300.11911 FAX: +39.2.300.11999 • JAPAN +81.3.5464.6411 FAX: +81.3.5464.6433 • SINGAPORE +65.788.6668 FAX: +65.788.0988
• SWEDEN +46.8.594.70590 FAX: +46.8.594.70581 • UK +44 191 514 8237 FAX: +44 1953 457 722 • USA: (401) 738-9150 FAX: (401) 738-4389

DIMENSIONS in inches



TYPICAL RANGE
R < 240Ω



TYPICAL RANGE
240Ω - 20KΩ

SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.070 x 0.070 ± 0.005 (1.781 x 1.781mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pad size	0.005 x 0.010 (0.127 x 0.254mm) minimum
Number of pads	2
Pad material	10kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

OPTIONS: Gold back for eutectic die attach
Gold bonding pads, 15kÅ minimum thickness
Consult Applications Engineer

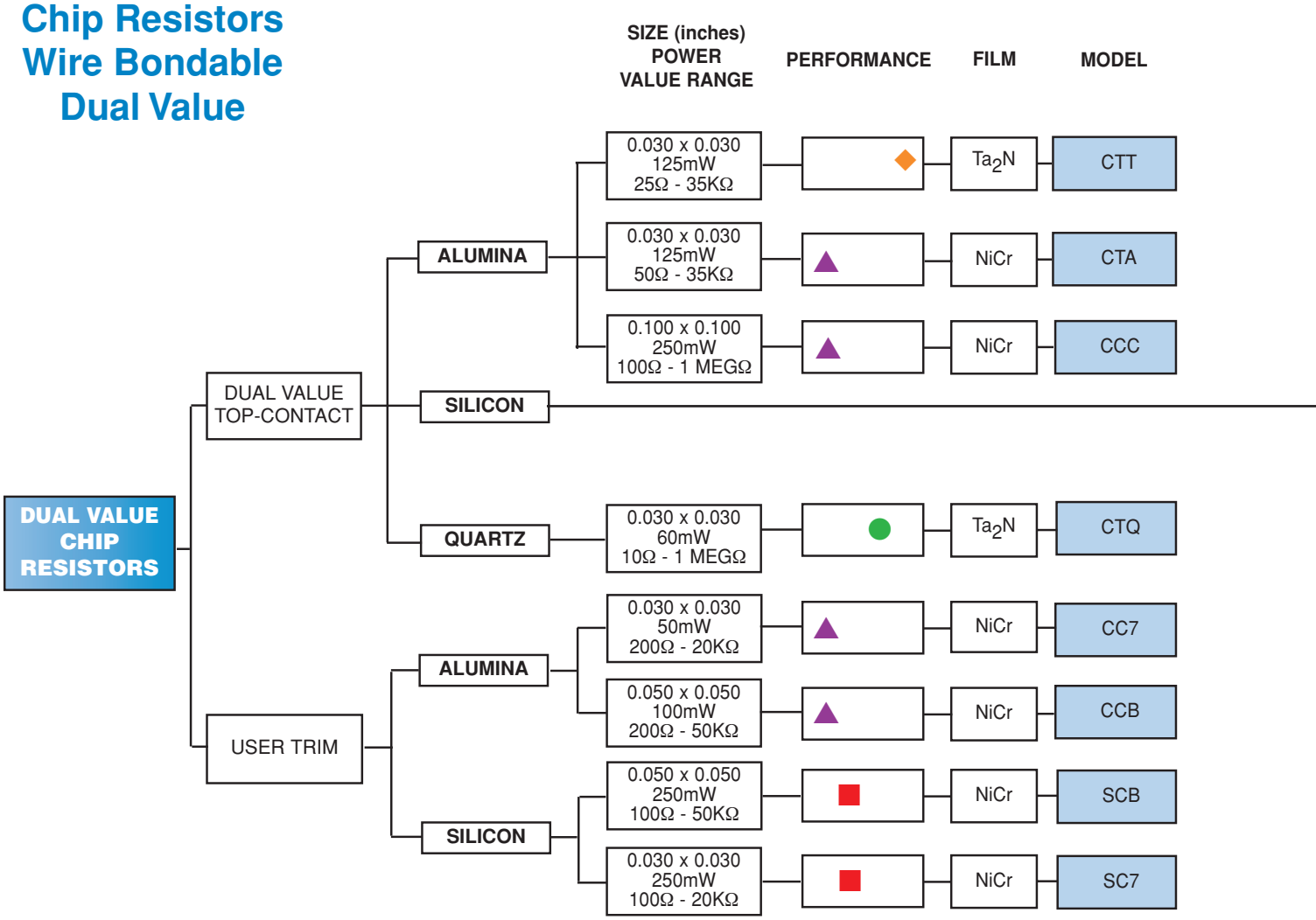
ORDERING INFORMATION

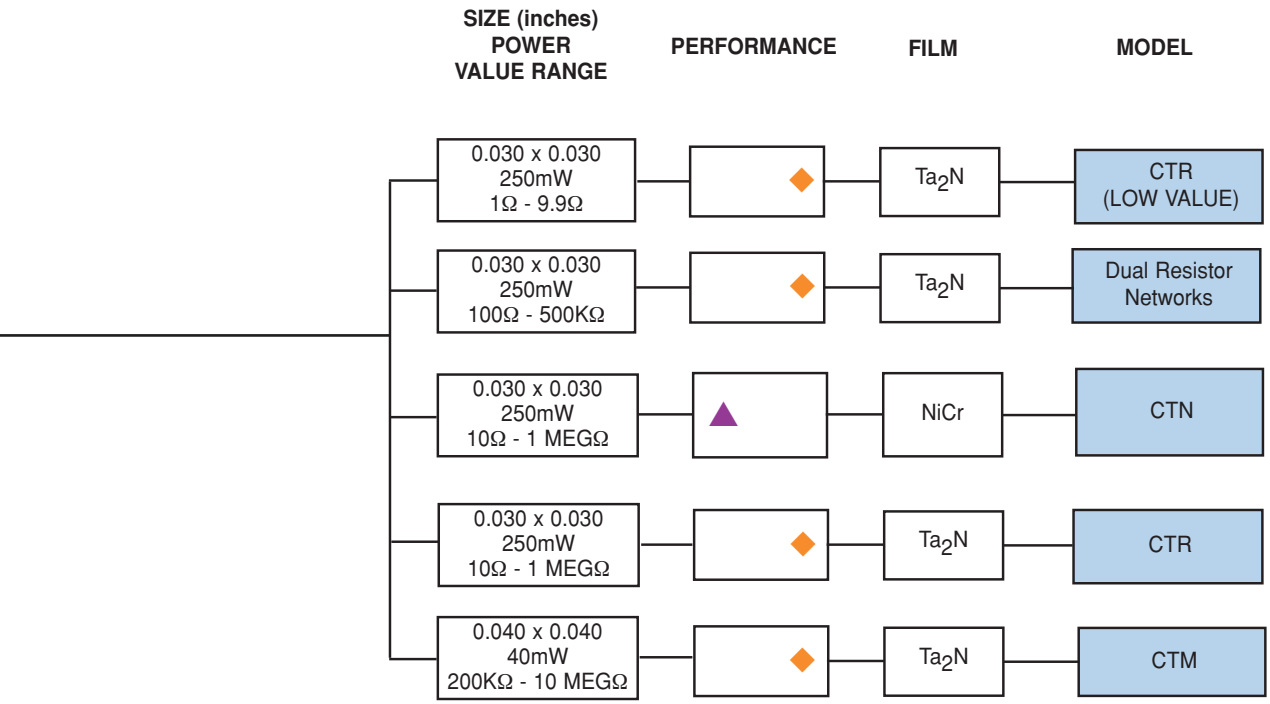
Example: 100% visual, 10kΩ, ± 1%, ± 100ppm/°C TCR, Aluminum Pads, Class H Visual inspection

W	**PWB**	**000**	**1000**	**1**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use first 4 digits significant digits of the resistance	**D** = 0.0001 **C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10	**D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

CHIP RESISTORS

Thin Film Chip Resistors Wire Bondable Dual Value





Performance Key

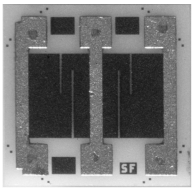
TCR	± 10ppm/°C
TOL	± 0.05%

TCR	± 25ppm/°C
TOL	± 0.1%

TCR	± 50ppm/°C
TOL	± 0.5%

TCR	± 100ppm/°C
TOL	± 1%

Thin Film, Center-Tapped Resistors



Product may not be to scale

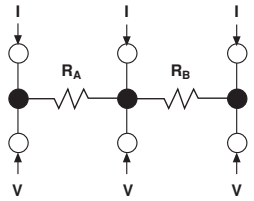
The CTT series resistor chips offer a combination of low shunt capacitance and excellent stability. The CTT offers the designer flexibility in use as either a single value resistor or as two resistor with a center tap feature.
The CTTs six bonding pads allows the user increased layout flexibility. The CTTs tantalum nitride resistor material offers excellent resistance to high moisture environments.
The CTTs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTTs are 100% electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

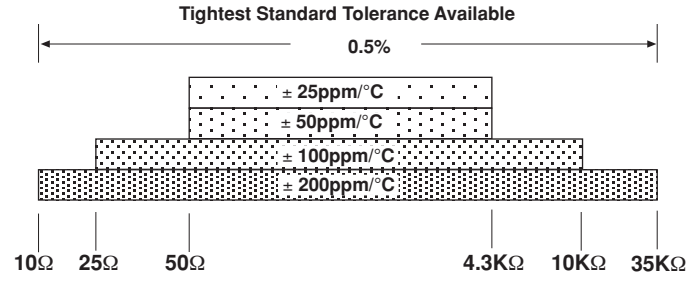
The CTT center-tapped resistor chips are used mainly in feedback circuits of amplifiers where ratio matching, tracking, low shunt capacitance and better frequency response are necessary.
Vishay EFI measures low-value resistors by the four-wire Kelvin technique.

FEATURES

- Center tap feature
- Chip size: 0.030 inches square
- Resistance range R_T: 10Ω to 36kΩ
- Alumina substrate, low shunt capacitance: < 0.2pF
- Resistor material: tantalum nitride
- Moisture resistant



TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
202	207
200	205
201	206
204	209

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
TCR tracking between halves ($R_A/R_{B)}$	± 2ppm/°C*
Center tap ratio, R_A/R_B: Tolerance	1 ± 1%
Noise, MIL-STD-202, Method 308	- 35dB typical
Moisture resistance, MIL-STD-202, Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 62mW	± 0.25% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.1% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.2% maximum ΔR/R
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at + 150°C)	125mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R%

*10ppm/°C for R < 100

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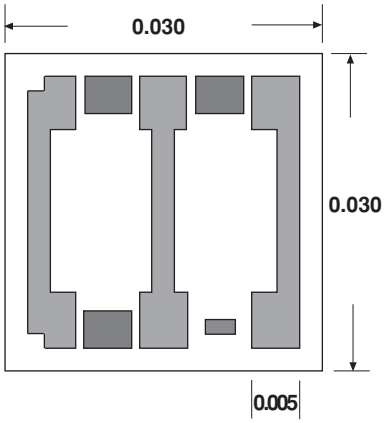
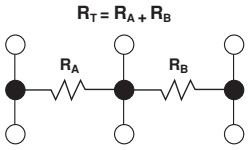
DIMENSIONS in inches



STANDARD CONFIGURATION
*Six locations. All pads 0.005 x 0.005

SCHEMATIC



MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.030 x 0.030 ± 0.002 (0.762 x 0.762 ± 0.050mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	99.6% Alumina
Resistor material	Tantalum nitride
Bonding pad size	0.005 x 0.005 (0.127 x 0.127mm)
Number of pads	6
Pad material	25kÅ minimum gold
Backing	None

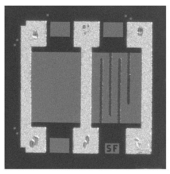
OPTIONS: Alphanumeric part marking, up to six characters
Aluminum bonding pads, 10kÅ minimum
Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 10kΩ, ± 1%, ± 100ppm/°C TCR, Gold Pads, Class H Visual inspection

W	**CTT**	**201**	**1000**	**1**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use first 4 digits significant digits of the resistance (R_T)	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000 **4** = 10000	**D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10% **M** = 20% **L** = 25%

Thin Film, Center-Tapped Resistors



Product may not be to scale

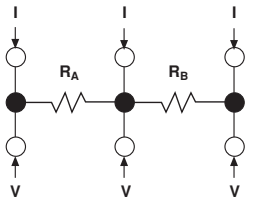
The CTA series resistor chips combine the best tolerances, stability and low shunt capacitance. The CTA offers the designer flexibility in use as either a single value resistor or as two resistors with a center tap feature. The CTAs six bonding pads allows the user increased layout flexibility. The CTAs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTAs are 100% electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

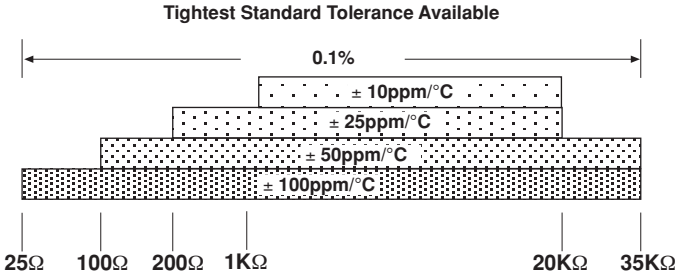
The CTA center-tapped resistor chips are used mainly in feedback circuits of amplifiers where ratio matching, low shunt capacitance and tracking between two resistors is critical.
Recommended for hermetic environments where chip is not exposed to moisture.
For lower values, the resistance of the six bonding-pad configurations can vary, depending on the method of measurement used. Vishay EFI measures low-value resistors by the four-wire Kelvin technique. The measuring method is illustrated in the diagram to the right.

FEATURES

- Center tap feature
- Tight ratio tolerances to: ± 0.1%
- Chip size: 0.030 inches square
- Resistance range total: 25Ω to 35kΩ
- Alumina substrate, low shunt capacitance: < 0.2pF
- Resistor material nichrome
- Excellent stability: ± 0.025% maximum ΔR/R



TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
203	233
202	232
200	230
201	231

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
TCR tracking between halves ($R_A/R_{B)}$)	± 2ppm/°C*
Center tap ratio, R_A/R_B: Tolerance	1 ± 1% standard
Noise, MIL-STD-202, Method 308	- 35dB typical
Moisture resistance, MIL-STD-202, Method 106, (Passivated only)	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 62mW	± 0.025% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.1% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.1% maximum ΔR/R
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at + 150°C)	125mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R%

*10ppm/°C for R < 100

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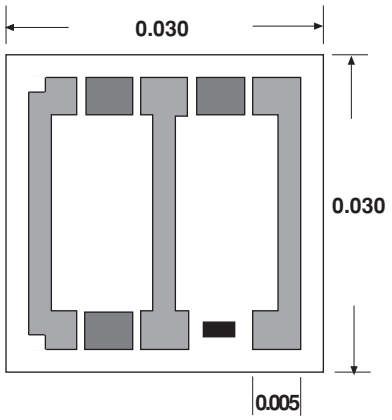
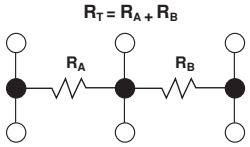
DIMENSIONS in inches



STANDARD CONFIGURATION
*Six locations. All pads 0.005 x 0.005

SCHEMATIC



MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.030 x 0.030 ± 0.002 (0.762 x 0.762 ± 0.050mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	99.6% Alumina
Resistor material	Nichrome
Bonding pad size	0.005 x 0.005 (0.127 x 0.127mm)
Number of pads	6
Pad material	25kÅ minimum gold
Backing	None

OPTIONS: Aluminum bonding pads, 10kÅ minimum
Center-tap ratio tolerances to 0.02% R > 1kΩ
Consult Applications Engineer

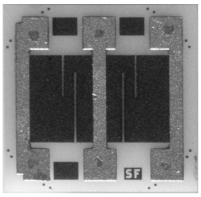
ORDERING INFORMATION

Example: 100% visual, 10kΩ, ± 1%, ± 100ppm/°C TCR, Gold Pads, Class H Visual inspection

W	**CTA**	**201**	**1000**	**1**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use first 4 digits significant digits of the resistance (R_T)	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10	**A** = 0.05% **B** = 0.1% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Vishay Electro-Films

Thin Film, 1010 Center-Tapped Resistors on Alumina



Product may not be to scale

The CCC series resistor chips offer good 400mw power, low shunt capacitance and a center tap feature.
The CCCs nichrome resistor material offers excellent stability.
The CCCs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology.
The CCCs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- Larger single size for extended value range
- Resistance range total: 100Ω to 1 MΩ
  Custom values: R_A or R_B - 50Ω to 500kΩ
- Power: 400mW
- Alumina substrate
- Low stray capacitance: < 0.2pF
- Resistor material: nichrome

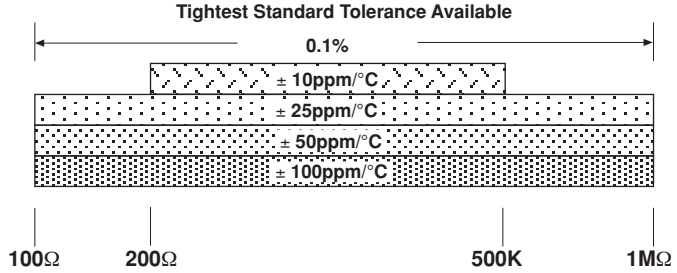
APPLICATIONS

Vishay EFI CCC chip resistors provide excellent high-frequency response and are ideally suited for prototyping.
Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

Recommended for hermetic environment where die is not exposed to moisture.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
203	207
200	204
201	205
202	206

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Center tap ratio, R_A/R_B: Tolerance	1 ± 1%
Stability, 1000 hours, + 125°C, 400mW	± 0.1% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.25% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	200V maximum
DC power rating at + 125°C	400mW maximum
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

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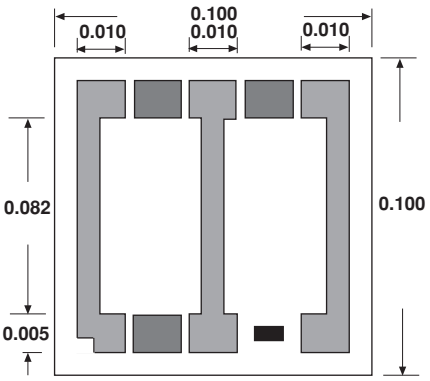
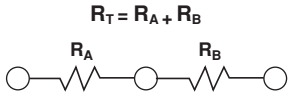
DIMENSIONS in inches



SCHEMATIC



MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.100 x 0.100 ± 0.003 (2.5 x 2.5 ± 0.08mm)
Chip thickness	0.010 ± 0.002 (0.25 ± 0.03mm)
Chip substrate material	99.6% alumina, 2-4 microinch finish
Resistor material	Nichrome
Bonding pad size	0.005 x 0.010 (0.12 x 0.24mm) minimum
Number of pads	6
Pad material	25kÅ minimum gold standard
Backing	None

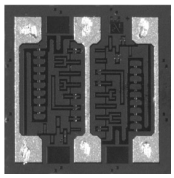
OPTIONS: Gold back for solder die attach
Contact Applications Engineer

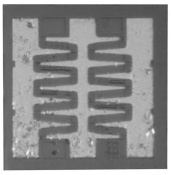
ORDERING INFORMATION

Example: 100% visual, R_T = 500Ω, 50Ω, ± 10%, ± 50ppm/°C TCR, $R_A = R_B = R_T/2$, Gold Pads, Class H Visual inspection
For tighter ratio tolerance, R_A,R_B or user trim consult factory for P/N.

W	**CCC**	**201**	**5000**	**A**	**K**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts X = Sample, visually inspected loaded in matrix trays (4% AQL)		See Process Code Table	Use first 4 significant digits of resistance (R_T)	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10	**B** = 0.1% **C** = 0.25% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Low Ohmic Value Resistors
Supplemental Data Sheet





Product may not be to scale

The CTR low ohm series provides a center tap option down to 1 ohm for non-critical tolerance applications.
The CTRs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTRs are 100% electrically tested and visually inspected to MIL-STD-883.

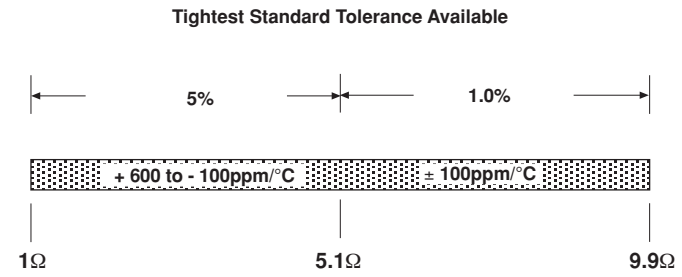
FEATURES

- Resistance range total: 1Ω to 9.9Ω
- Center Tap
- Chip size: 0.030 inches square
- Oxidized silicon substrate for good power dissipation
- Resistor material: Tantalum nitride, self passivating

APPLICATIONS

For low values, the resistance of the six bonding pad configurations can vary, depending on the method of measurement used. Vishay EFI measures low value resistors by the four-wire kelvin technique using the method illustrated in the measurement schematic for resistors of less than 10.
Consult Vishay EFI Applications Engineering for alternate measurement method if tighter requirements are needed.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
101	131

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
TCR tracking between halves (R_A/R_B)	± 200ppm/°C typical
Voltage ratio, R_A/R_B: Tolerance	1 ± 5%
Noise, MIL-STD-202, Method 308	- 20dB typical
Stability, 1000 hours, + 125°C, 125mW	± 0.25% ± 0.01% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.1% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.2% + 0.01% maximum ΔR/R
DC power rating at + 70°C (derated to zero at 175°C)	250mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.1% maximum ΔR/R

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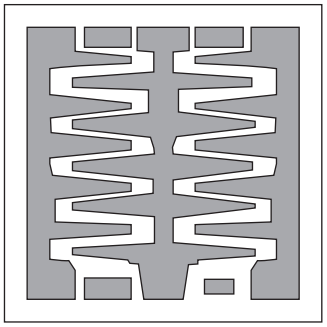
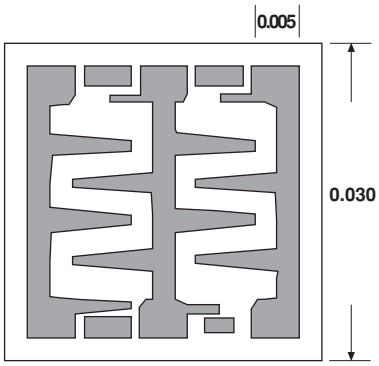
DIMENSIONS in inches

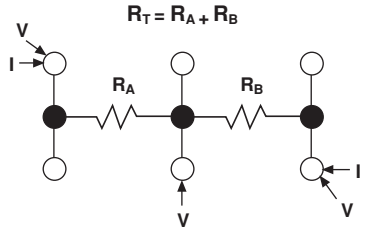


TYPICAL RANGE
1Ω - 6.7Ω



TYPICAL RANGE
6.8Ω - 9.9Ω

SCHEMATIC



MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.030 x 0.030 ± 0.002 (0.762 x 0.762 ± 0.05mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum Nitride, self-passivating
Bonding pad size	0.005 x 0.005 (0.127 x 0.127mm) minimum
Number of pads	6
Pad material	10kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

OPTIONS: Alphanumeric part parking, up to six character
Gold bonding pads, 15kÅ minimum;
Contact Applications Engineer

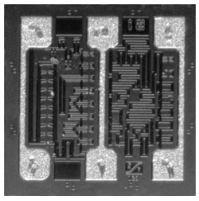
ORDERING INFORMATION

Example: 100% visual, 2Ω, ± 5%, + 600 to - 100ppm/°C TCR, Aluminum Pads, Class H Visual inspection

W	**CTR**	**101**	**2000**	**C**	**J**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts X = Sample, visually inspected loaded in matrix trays (4% AQL)		See Process Code Table	Use first 4 significant digits of resistance (R_T)	**D** = 0.0001 **C** = 0.001 **B** = 0.01	**F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Vishay Electro-Films

Dual Resistor Divider Thin Film Custom Network



Product may not be to scale

The STR, DTR series of dual resistor dividers provides the user with the option to specify the value, tolerance of each individual resistor and ratio tolerance.
The dual resistor dividers are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The dual resistor dividers are 100% electrically tested and visually inspected to MIL-STD-883.

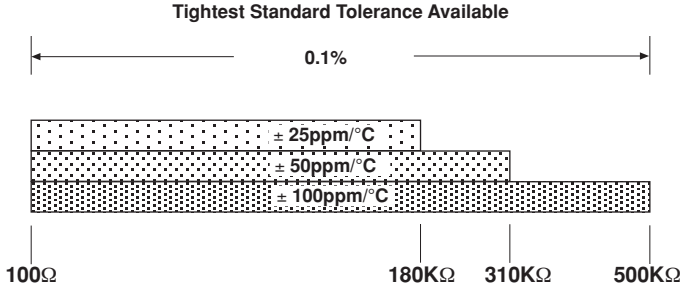
FEATURES

- Individual value and tolerance selection
- Ratio tolerance to 0.05%
- Chip size: 0.030 inches square
- Resistance range: 100Ω to 500kΩ
- Oxidized silicon substrate for good power dissipation
- Resistor material: tantalum nitride, self-passivating

APPLICATIONS

Vishay EFI custom-made two resistor chips are designed for hybrid packages requiring close ratio-matching and tracking of two different resistors for gain accuracy and stability. The customized resistance values give the hybrid designer greater flexibility.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



Resistance range refers only to R_A or R_B
Extended value/TCR range available using Nichrome version

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
TCR tracking between halves (R_A/R_B)	± 10ppm/°C, (R_A < 1K) ± 5ppm/°C, (R_A ≥ 1K)
Resistance ratio tolerance R_A/R_B	Customer specified to 0.05%
Noise, MIL-STD-202, Method 308 100Ω - 250kΩ < 100Ω or > 251kΩ	 - 35dB typical - 20db typical
Moisture resistance, MIL-STD-202, Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C derated power	± 0.2% maximum absolute ± 0.02 maximum ratio
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.1% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.2% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V
DC power rating at + 70°C (derated to zero at 175°C)	125mW each resistor
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.1% maximum ΔR/R

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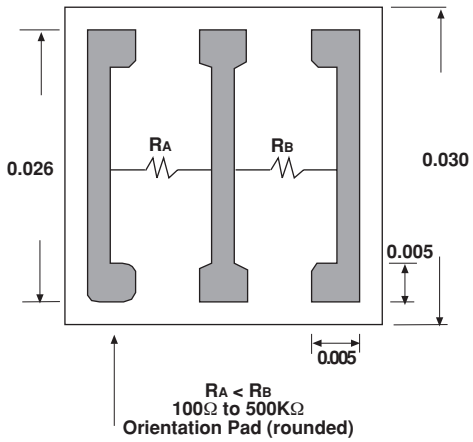
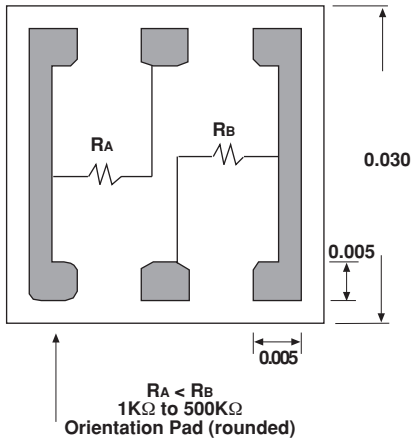
DIMENSIONS in inches

STR SERIES CONFIGURATION



DTR SERIES CONFIGURATION



SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.030 x 0.030 ± 0.003 (0.762 x 0.762 ± 0.05mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum Nitride, self-passivating
Bonding pad size	0.005 x 0.005 (0.127 x 0.127mm) minimum
Number of pads	6
Pad material	10kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

OPTIONS: Gold back for eutectic die attach
Gold bonding pads, 15kÅ minimum;
Contact Applications Engineer

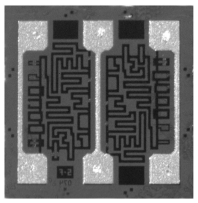
ORDERING INFORMATION

Example: 100% visual, STR format, 1kΩ/20kΩ, 1% Tolerance, 0.1% Ratio, 50ppm/°C, Aluminum Pads, Class H Visual inspection

W	STR	1000	0 /	2000 1	F	B	D	H	A
INSPECTION /PACKAGING	PRODUCT FAMILY	RESISTANCE VALUE (R_1)	MULTIPLIER CODE	RESISTANCE VALUE + MULTIPLIER (R_2)	TOLERANCE CODE	RATIO TOLERANCE	TCR	CLASS	BOND PADS
W = 100% visually inspected parts per MIL-STD-883 X = Sample, visually inspected loaded in matrix trays (4% AQL)		Use first 4 digits	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000		**B** = 0.01% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%	**D** = 0.05% **F** = 0.1% **G** = 0.2% **J** = 0.5% **K** = 1% **M** = 2%	**B** = ± 25 **D** = ± 50 **E** = ± 100 **G** = ± 200	Class H Class K	Aluminum Gold

Vishay Electro-Films

Nichrome Thin Film, Center Tapped Resistors



Product may not be to scale

The CTN series is a center tapped nichrome resistor chip providing excellent stability at 250mW power levels. The CTN offers the designer flexibility in use as either a single value resistor or as two resistors with a center tap feature. The CTNs six bonding pads allows the user increased layout flexibility.

The CTNs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTNs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- Center tap feature
- Chip size: 0.030 inches square
- Resistance range total: 10Ω to 1MΩ
- Ratio tolerances to: 0.1%
- Resistor material: nichrome
- Oxidized silicon substrate for good power dissipation

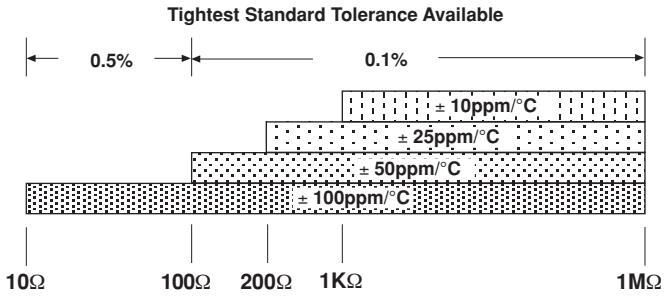
APPLICATIONS

The CTN center-tapped resistor chips are used mainly in feedback circuits of amplifiers where ratio matching, high power and tracking between two resistors is critical.

Recommended for Hermetic environment where die is not exposed to moisture.

For low values, the resistance of the six bonding-pad configurations can vary, depending on the method of measurement used. Vishay EFI measures low-value resistors by the four wire Kelvin technique.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
203	263
202	262
200	260
201	261

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
TCR tracking between halves (R_A/R_B)	± 2ppm/°C*
Center tap ratio, R_A/R_B tolerance	1 ± 1% standard
Noise, MIL-STD-202, Method 308, 100Ω - 250kΩ	- 35dB typical
Stability, 1000 hours, + 125°C, 125mW	± 0.1% ΔR/R
Operating temperature range	- 55°C to + 125°C
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at + 175°C)	250mW

*20ppm/°C for R < 20

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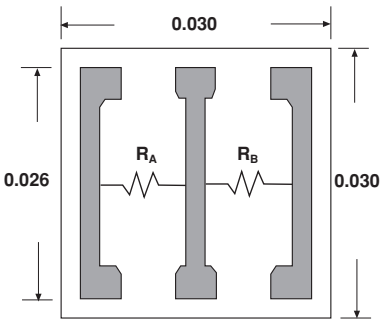
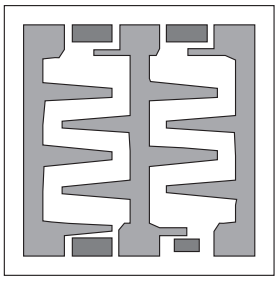
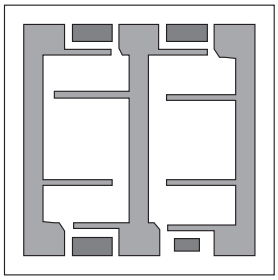
CONFIGURATIONS in inches



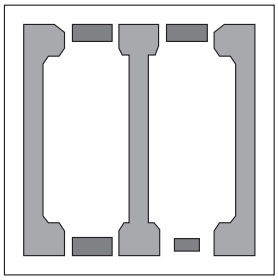
STANDARD CONFIGURATION
Six locations. All pads 0.005 x 0.005 inch



TYPICAL RANGE
10Ω - 49Ω

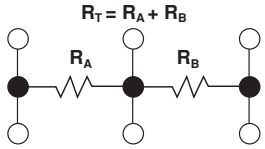


TYPICAL RANGE
50Ω - 199Ω



TYPICAL RANGE
100Ω - 1MΩ

SCHEMATIC



MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip size	0.030 x 0.030 ± 0.002 (0.762 x 0.762 ± 0.05mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Nichrome
Bonding pad size	0.005 x 0.005 (0.127 x 0.127mm) minimum
Number of pads	6
Pad material	15kÅ minimum gold standard
Backing	None, lapped semiconductor silicon

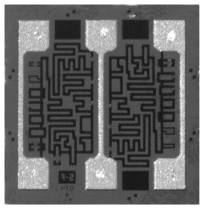
OPTIONS: Alphanumeric part marking, up to six characters
Gold backing for eutectic die attach
Center tap ratio tolerances to 0.01%
Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 10kΩ, ± 1%, ± 100ppm/°C TCR, Gold Pads, Class H Visual inspection

W	**CTN**	**201**	**1000**	**1**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrixtrays (4% AQL)		See Process Code Table	Use first 4 significant digits of resistance (R_T)	**C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000 **4** = 10000	**B =** 0.1% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Thin Film, Center-Tapped Resistors

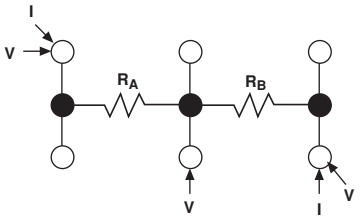


Product may not be to scale

The CTR series is a center-tapped resistor chip combining excellent stability with 250mW power levels. The CTR offers the designer flexibility in use as either a single value resistor as two resistors with a center tap feature. The CTR's six bonding pads allows the user increased layout flexibility.
The CTRs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTRs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

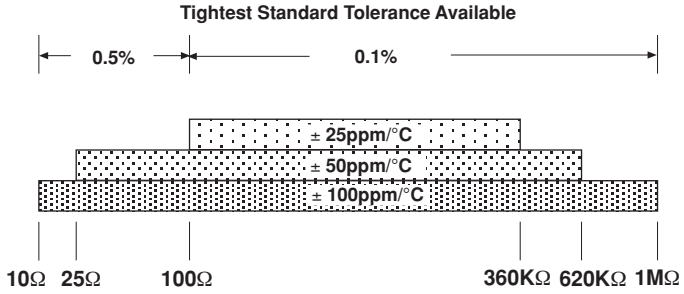
- Center tap feature
- Tight ratio tolerances to: 0.05%
- Chip size: 0.030 inches square
- Resistance range total: 10Ω to 1MΩ
- Oxidized silicon substrate for good power dissipation
- Resistor material: tantalum nitride, self-passivating
- Moisture resistant



APPLICATIONS

Vishay EFI CTR center-tapped resistor chips are used mainly in feedback circuits of amplifiers where ratio matching, high power and tracking between two resistors is critical.
For low values, the resistance of the six bonding-pad configurations can vary, depending on the method of measurement used. Vishay EFI measures low-value resistors by the four wire Kelvin technique. The method illustrated above is critical for resistors of less than 100Ω.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
102	132
100	130
101	131

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
TCR tracking between halves (R_A/R_B)	± 2ppm/°C*
Center tap ratio, R_A/R_B tolerance	1 ± 1% standard
Noise, MIL-STD-202, Method 308, < 100Ω or > 251kΩ	- 20dB typical
Moisture resistance, MIL-STD-202, Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 125mW	± 0.2% maximum absolute
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.1% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.2% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at + 175°C)	250mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.1% maximum ΔR/R

*5ppm/°C for R < 100
20ppm/°C for R < 20

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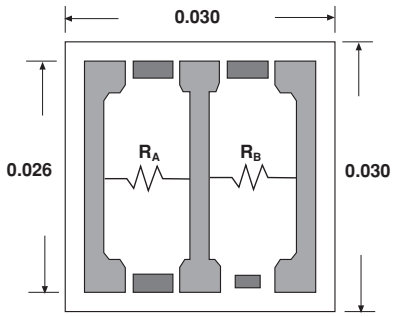
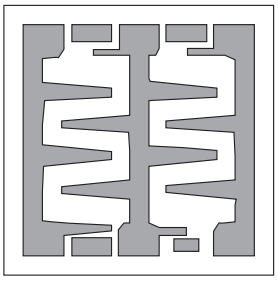
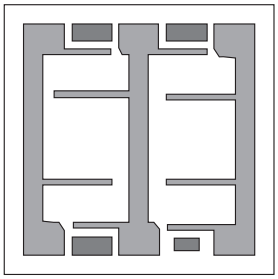
CONFIGURATIONS in inches



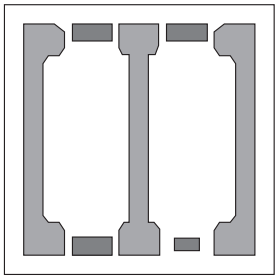
STANDARD CONFIGURATION
Six locations. All pads 0.005 x 0.005 inch



TYPICAL RANGE
10Ω - 26.9Ω

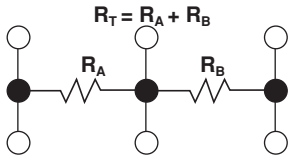


TYPICAL RANGE
27Ω - 99Ω



TYPICAL RANGE
100Ω - 1MΩ

SCHEMATIC



MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip size	0.030 x 0.030 ± 0.002 (0.762 x 0.762 ± 0.05mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum nitride, self passivating
Bonding pad size	0.005 x 0.005 (0.127 x 0.127mm)
Number of pads	6
Pad material	10kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

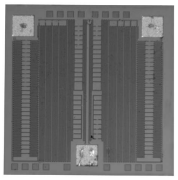
OPTIONS: Alphanumeric part marking, up to six characters
Gold bonding pads 15kÅ minimum; Ratio Tolerance to 0.05%
1 to 10 ohm values available, See CTR Low Ohm
Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 10kΩ, ± 1%, ± 100ppm/°C TCR, Aluminum Pads, Class H Visual inspection

W	**CTR**	**101**	**1000**	**1**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrixtrays (4% AQL)		See Process Code Table	Use first 4 significant digits of resistance (R_T)	**C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000 **4** = 10000	**A** = 0.05% **B** = 0.1% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Megohm Center-Tap Chip Resistor



Product may not be to scale

The CTM resistor chips extends the resistance range to 10Meg in a center tap configuration while keeping the die size relatively small.
The CTMs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTMs are 100% electrically tested and visually inspected to MIL-STD-883.

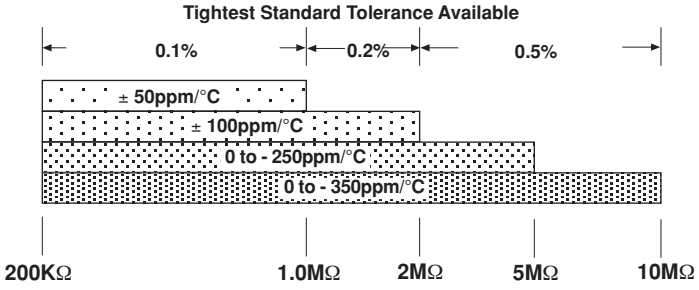
FEATURES

- Resistance range total: 200kΩ to 10MΩ
- Center Tap
- Chip size: 0.040 inches square
- Resistor material: tantalum nitride, self-passivating
- Moisture resistant

APPLICATIONS

Vishay EFI CTM tapped megohm resistor chips are designed for hybrid packages requiring high value, two resistor combinations.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
100	130
101	131
099	129
098	128

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
TCR tracking between resistors	± 5ppm/°C
Ratio/ratio, R_A/R_B: Tolerance	1 ± 1% standard
Noise	- 12dB typical
Moisture resistance, MIL-STD-202, Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 10mW	± 0.5% maximum absolute ± 0.005% ratio
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at + 175°C)	20mW each resistor
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R%

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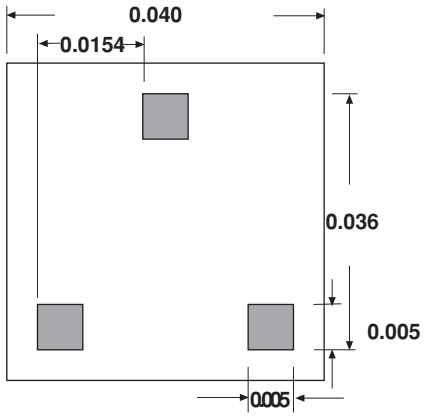
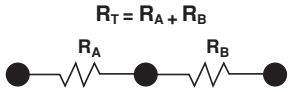
DIMENSIONS in inches



SCHEMATIC



MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.040 x 0.040 ± 0.002 (1.02 x 1.02 ± 0.05mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pad size	0.005 x 0.005 (0.127 x 0.127mm)
Number of pads	3
Pad material	10kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

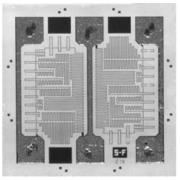
OPTIONS: Gold back for eutectic die attach
Custom Ratios available up to 4:1 R_A/R_B - Consult Vishay EFI Sales
Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 2MΩ, ± 1%, ± 100ppm/°C TCR, Aluminum Pads, Class H Visual inspection

W	**CTM**	**101**	**2000**	**3**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use first 4 digits significant digits of the resistance (R_T)	**2** = 100 **3** = 1000 **4** = 10000	**B** = 0.1% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Thin Film Center-Tapped Resistors



Product may not be to scale

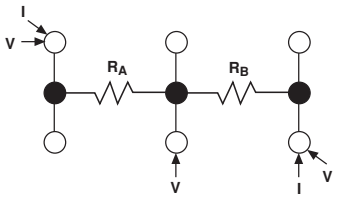
The CTQ series resistor chips offer a wide resistance range with lower shunt capacitance than can be offered with the silicon based resistors but only at a lower power level.
The CTQ offers the designer flexibility in use as either a single value resistor or as two resistor with a center tap feature. The CTQs six bonding pads allows the user increased layout flexibility.
The CTQs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTQs are 100% electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

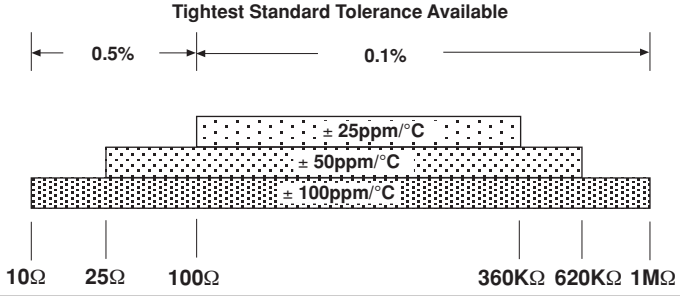
The CTQ center-tapped resistor chips are used mainly in feedback circuits of amplifiers where ratio matching, low shunt capacitance and tracking between two resistors is critical.
For low values, the resistance of the six bonding pad configuration can vary, depending on the method of measurement used. Vishay EFI measures low-value resistors by the four-wire Kelvin technique.

FEATURES

- Center tap feature
- Chip size: 0.030 inches square
- Resistance range total: 10Ω to 1MΩ
- Resistor material: Tantalum nitride, self-passivating
- Moisture resistant
- Quartz substrate
- Low shunt capacitance < 0.1pF



TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
102	132
100	130
101	131

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
TCR tracking between halves (R_A,R_B)	± 2ppm/°C*
Center tap ratio, R_A/R_B: Tolerance	1 ± 1% standard
Noise, MIL-STD-202, Method 308, 100Ω - 250kΩ < 100Ω or > 251kΩ	- 35dB typical - 20db typical
Moisture resistance, MIL-STD-202, Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 30mW	± 0.25% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.1% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.2% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	200V
DC power rating at + 70°C (derated to zero at + 175°C)	60mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R%

*5ppm/°C for R < 100. 20ppm/°C for R < 20

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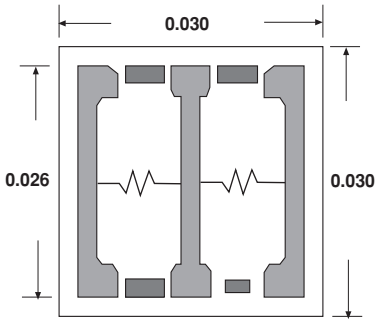
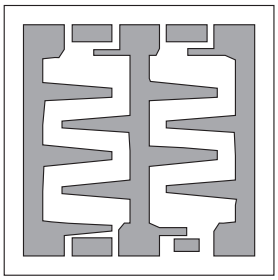
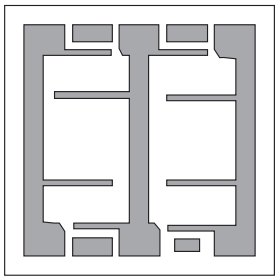
DIMENSIONS in inches



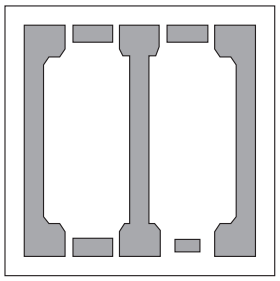
STANDARD CONFIGURATION
Six locations. All pads 0.005 x 0.005 inches



TYPICAL RANGE
10Ω - 26.9Ω

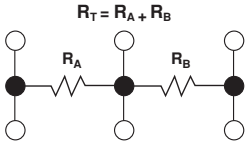


TYPICAL RANGE
27Ω - 99Ω



TYPICAL RANGE
100Ω - 1MΩ

SCHEMATIC



MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip size	0.030 x 0.030 ± 0.002 (0.762 x 0.762 ± 0.05mm)
Chip thickness	0.010 ± 0.003 (0.254 ± 0.05mm)
Chip substrate material	Quartz
Resistor material	Tantalum nitride, self-passivating
Bonding pad size	0.005 x 0.005 (0.127 x 0.127mm)
Number of pads	6
Pad material	10kÅ minimum aluminum
Backing	None, lapped quartz

OPTIONS: Alphanumeric part marking, up to six characters
Gold bonding pads, 15kÅ minimum
Center-tap ratio tolerances to 0.05%
1 to 10 ohm values available
Contact Applications Engineer

ORDERING INFORMATION

Example: 100% visual, 10kΩ, ± 1%, ± 100ppm/°C TCR, Aluminum Pads, Class H Visual inspection

W	**CTQ**	**101**	**1000**	**1**	**F**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4% AQL)		See Process Code Table	Use first 4 digits significant digits of the resistance (R_T)	**D** = 0.0001 **C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000 **4** = 10000	**B** = 0.1% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

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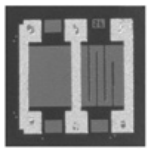
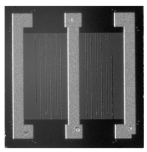
Thin Film Resistors on Alumina, User Trimmable





Product may not be to scale

The CC7 and CCB series resistor chips offer the combination of user trimmability, low shunt capacitance and excellent stability. The CC7 and CCB can be specified as either a single R_T value resistor, as two resistors with a center tap feature (1:1 ratio or custom) ratio or user trimmable.
The CC7 and CCBs a six bonding pads allows the user increased layout flexibility. The CC7 and CCBs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. They are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- Small single chip size
  CC7 - 0.030 inches square
  CCB - 0.050 inches square
- Alumina substrate
- Low stray capacitance: < 0.2pF
- Resistance range R_T: 100Ω to 20kΩ for CC7
  Resistance range R_T: 100Ω to 50kΩ for CCB
- Resistor material: nichrome
- User trimmable

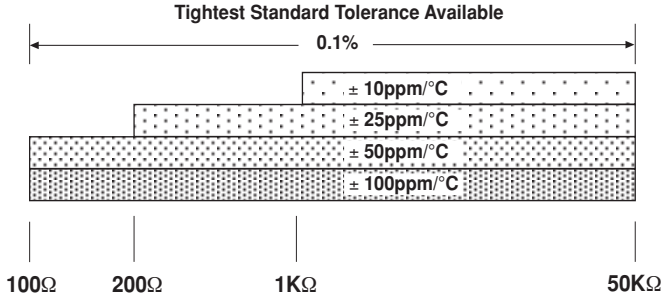
APPLICATIONS

Vishay EFI CC7 and CCB chip resistors provide excellent high frequency response and are ideally suited for prototyping. Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

Recommended for hermetic environments where die is not exposed to moisture

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE			
CC7		CCB	
CLASS H*	CLASS K*	CLASS H*	CLASS K*
219	223	219	223
220	224	220	224
221	225	221	225
222	226	222	226

*MIL-PRF-38534 inspection criteria
R_A user trimmable 50% above
R_T value specified in P/N

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Stability, 1000 hours, + 125°C at rated power	+ 0.1% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	+ 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	+ 0.25% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at 125°C	50mW maximum (30 mil) 100mW maximum (50 mil)
5 x rated power short-time overload, + 25°C, 5 seconds	+ 0.25% maximum ΔR/R

NOTE: Performance characteristics are not guaranteed once user trimmed

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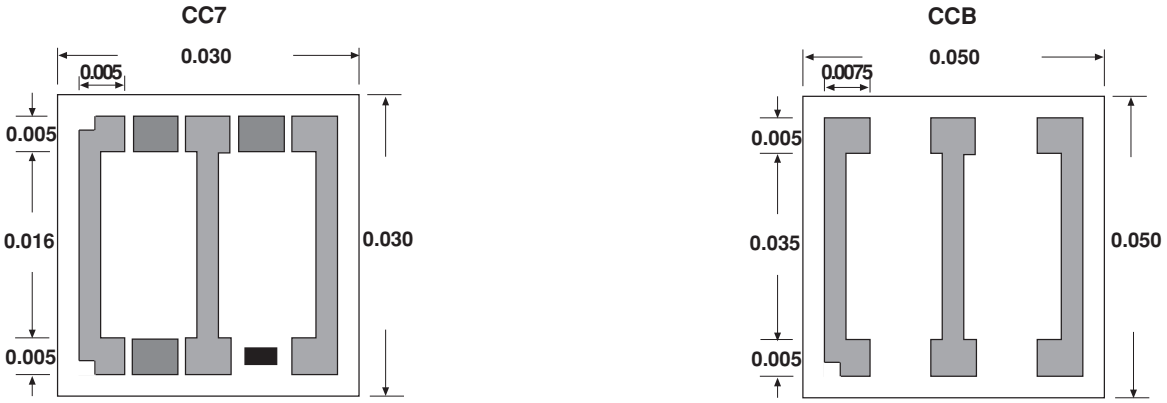
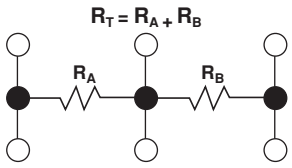
DIMENSIONS in inches



SCHEMATIC



MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.030 x 0.030 ± 0.003 (0.76 x 0.76 ± 0.08mm) 0.050 x 0.050 ± 0.003 (1.27 x 1.27 ± 0.08mm)
Chip thickness	0.010 ± 0.002 (0.25 ± 0.03mm)
Chip substrate material	99.6% alumina, 2 - 4 microinch finish
Resistor material	Nichrome
Bonding pad size	0.005 x 0.005 (0.12 x 0.12mm) minimum
Number of pads	6
Pad material	25kÅ minimum gold standard
Backing	None

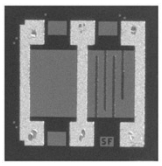
OPTIONS: Gold back for solder die attach
Consult Application Engineer

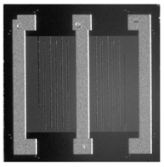
ORDERING INFORMATION

Example: 100% visualled, R_T = 500, ± 10%, ± 50ppm/°C TCR, Gold pads, Class H vixual inspection, 30 mil size, R_A user trim.
Standard user trim versions will be supplied with R_A untrimmed
For custom R_A, R_B combinations consult Application Engineer

W	**CC7**	**221**	**5000**	**A**	**K**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts X = Sample, visually inspected parts loaded in matrix trays (4% AQL)	CC7 CCB	See Process Code Table	Use first 4 digits significant digits of the resistance (R_T)	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10	**B** = 0.1% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Thin Film Resistors on Silicon, User Trimmable





Product may not be to scale

The SC7 and SCB series resistor chips offer a combination of nichrome user trimmability as a single resistor or as a ratio trim while maintaining the excellent TCR tracking characteristics of two resistors on the same chip.
The SC7 and SCBs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The SC7 and SCBs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- Chip sizes

  SC7 - 0.030 inches square
  SCB - 0.050 inches square

- Resistance range R_T: 100Ω to 20kΩ for SC7
  Resistance range R_T: 100Ω to 50kΩ for SCB
- Silicon substrate
- Power: 250 or 400mW capability
- Resistor material: nichrome
- User trimmable

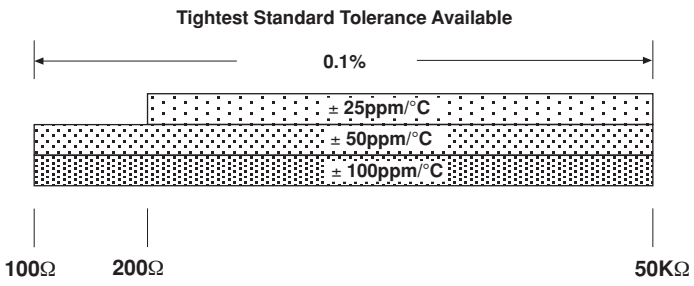
APPLICATIONS

Vishay EFI SC7 and SCB chip resistors have excellent power dissipation capability and are ideally suited for prototyping. Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

Recommended for hermetic environments where die is not exposed to moisture

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE			
SC7		SCB	
CLASS H*	CLASS K*	CLASS H*	CLASS K*
220	224	220	224
221	225	221	225
222	226	222	226

*MIL-PRF-38534 inspection criteria
R_A user trimmable 50% above
R_T value specified in P/N

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Stability, 1000 hours, + 125°C at rated power	± 0.2% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 100 hours	± 0.25% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at 70°C Derated to zero at 150°C	250mW maximum (0.030 inches) 400mW maximum (0.050 inches)
5 x rated power short-time overload, + 25°C, 5 seconds	+ 0.25% maximum ΔR/R

NOTE: Performance characteristics are not guaranteed once user trimmed

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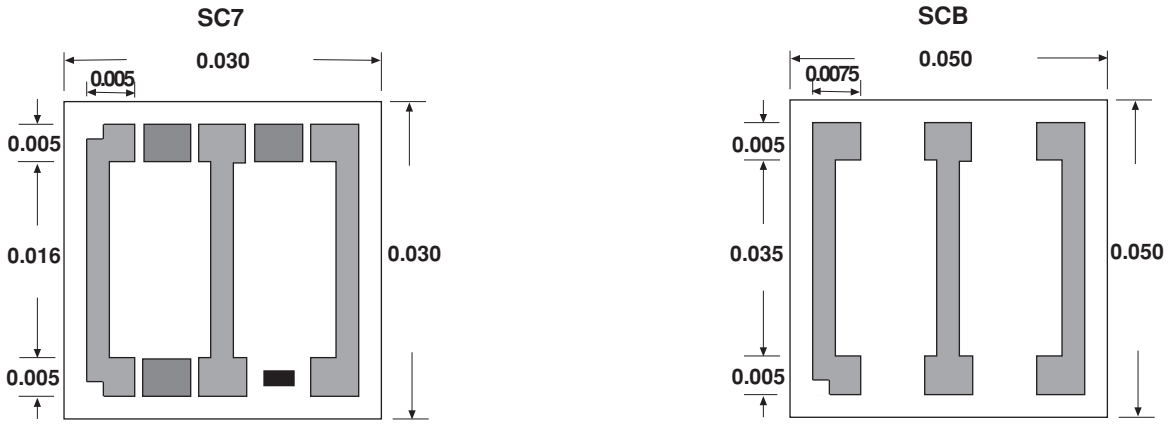
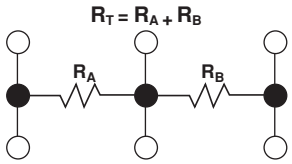
DIMENSIONS in inches



SCHEMATIC



MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.030 x 0.030 ± 0.003 (0.76 x 0.76 ± 0.076mm) 0.050 x 0.050 ± 0.003 (1.27 x 1.27 ± 0.076mm)
Chip thickness	0.010 ± 0.002 (0.25 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Nichrome
Bonding pad size	0.005 x 0.005 (0.127 x 0.127mm) minimum
Number of pads	6
Pad material	15kÅ minimum gold standard
Backing	None, lapped semiconductor silicon

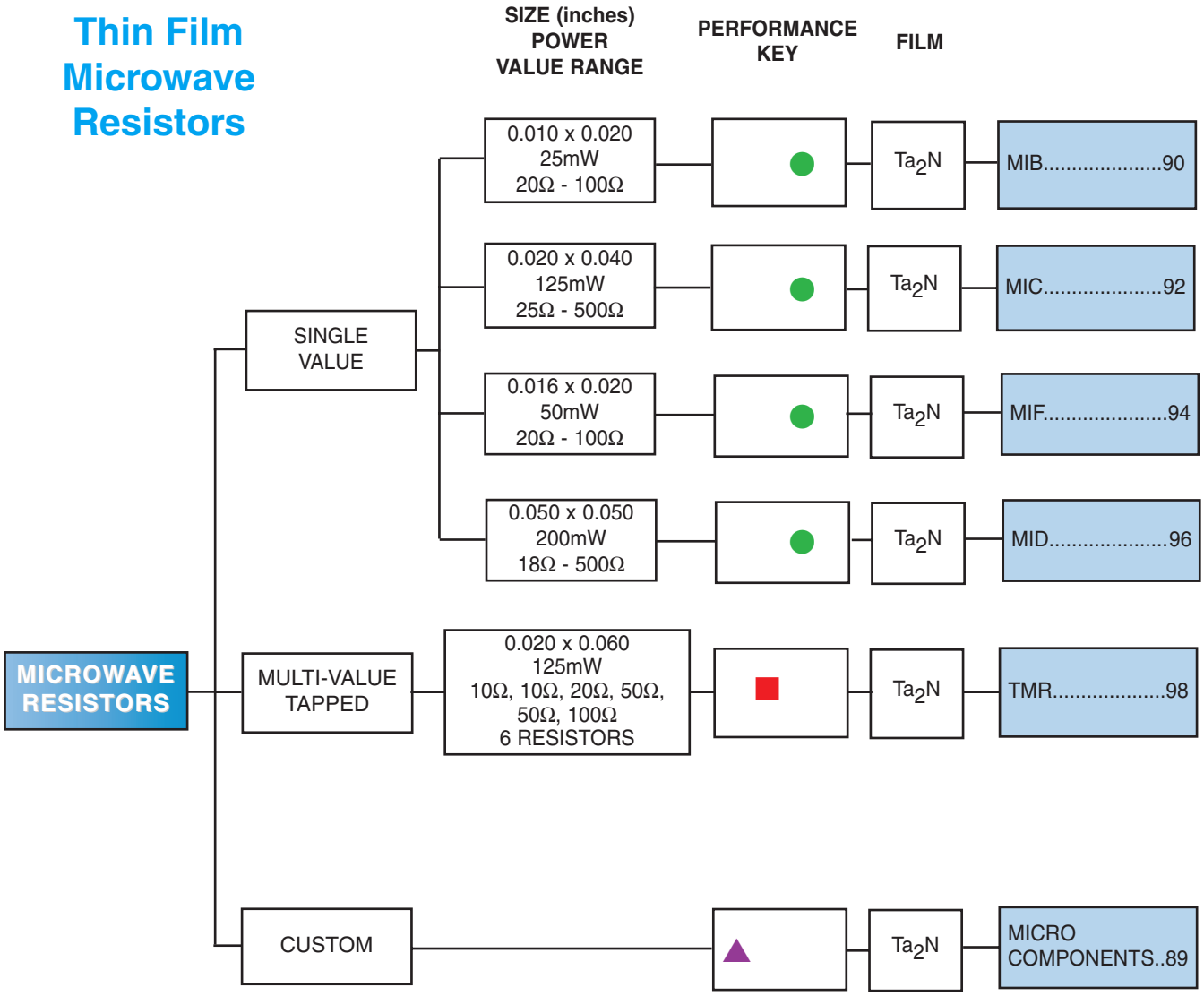
OPTIONS: Gold back for solder die attach
Consult Application Engineer

ORDERING INFORMATION

Example: 100% visualled, R_T = 500, ± 10%, ± 50ppm/°C TCR, R_A user trim Gold pads, Class H visual inspection
Standard user trim versions will be supplied with R_A untrimmed
For custom R_A, R_B combinations consult Application Engineer

W	**SC7**	**221**	**5000**	**A**	**K**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)	SC7 SCB	See Process Code Table	Use first 4 digits significant digits of the resistance (R_T)	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10	**B** = 0.1% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10% **M** = 20%

Thin Film Microwave Resistors

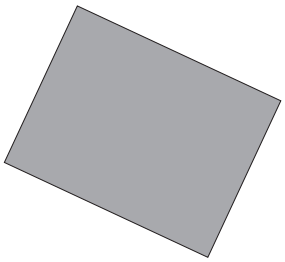


Performance Key

▲		■		●	
TCR	± 50ppm/°C	TCR	+ 100ppm/°C	TCR	± 200ppm/°C
TOL	± 0.1%	TOL	± 1%	TOL	± 1%

Thin Film Microwave Components

METALIZED PLATES



Product may not be to scale

Vishay Electro-Films (EFI) offers a wide variety of metalized substrates suitable for microwave hybrid and microwave integrated circuit applications. Vishay EFI's unique economical fabrication process provides an exceptional range of dimensions, metalizations and circuitry. Typical applications include: amplifiers, oscillators, limiters, couplers filters, attenuators with frequency response through 18gHz and into the millimeter wavelength range.

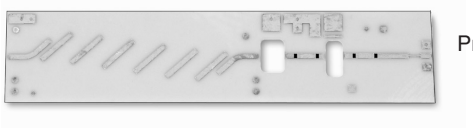
SUBSTRATE MATERIAL

- Alumina (as fired or polished) standard thicknesses of 0.010 inches, 0.015 inches and 0.025 inches, dielectric constant 9.8 typical @ 25°C - 10gHz
  Loss factor 0.004 typical @ 25°C - 10gHz
- Quartz - Beryllium Oxide various thicknesses
- Sizes - up to 4.1 inches x 3.3 inches

METALIZATION

- Sputtered in various combinations of NiCr, Ta_2N, Ni, Au, Al, TiW, Ti, Pd
- Electroplated - Cu, Ni, Au up to 300 microinches
- Excellent adhesion (typically 7 - 10,000 lbs./inches square)
- One, two or six surfaces
- Through Holes - metalized or non-metalized

PATTERNED & ETCHED SUBSTRATES

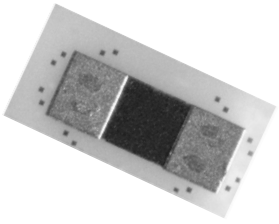


Product may not be to scale

Vishay EFI can handle the transition from a circuit requirement to a finished thin film microcomponent with in-house artwork and photo mask generation. Vishay EFI's processing techniques and quality control guarantee optimum quality in prototype or production quantities. Vishay EFI is a thin film specialist with unequalled productivity.

- Conductor only or resistor/conductor patterns
- Resistive films - high stability Nichrome or self-passivating Ta_2N
- In-house laser machining for round or odd shaped substrates
- Metalized through holes
- Patterned edges
- Planar inductors
- Large couplers with fine line patterns, line and space tolerances as ± 50 microinches

PRECISION CHIP RESISTORS

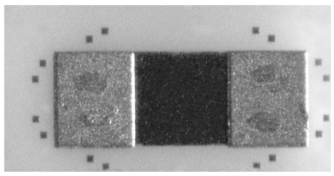


Product may not be to scale

Vishay EFI precision chip resistors are edge trimmed to tolerance providing excellent high frequency response. Edge trimming leaves a solid symmetrical block resistor void of any laser cuts eliminating the capacitive effects from a plunge "L" cut trim.

- Attenuator chips
- Resistance range 20Ω to 1MΩ
- Automatic laser trimming to ± 0.05% absolute
- Edge trim for high frequency applications
- Gold or solder coated terminations
- TCR ± 50ppm/°C, ± 25ppm/°C or ± 10ppm/°C
- Single side or wraparound terminations
- Size - 0.020 inches x 0.040 inches to 0.100 inches x 0.100 inches

Thin Film Microwave Resistor



Product may not be to scale

The MIB resistor chips on alumina are designed with low shunt capacitance. Resistor geometrics are compatible with strip lines, making them ideally suited for microwave circuits. These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The MIBs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- Small single chip size: 0.010 x 0.020 inches
- Microwave resistance range: 20Ω to 100Ω
- Overall resistance range: 20Ω to 2kΩ
- Alumina substrate
- Low stray capacitance: < 0.2pF
- Resistor material: tantalum nitride, self passivating
- Moisture resistant

APPLICATIONS

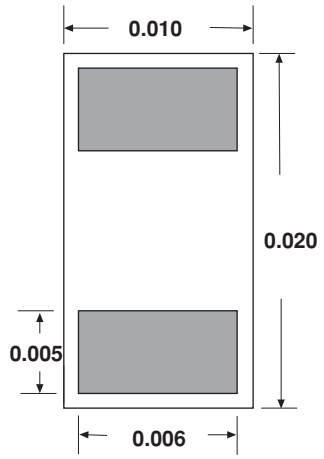
Vishay EFI MIB chip resistors provide excellent high-frequency response and are ideally suited for prototyping. Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES	
Resistance Range	20Ω to 100Ω
Tolerance	± 5%, ± 10%, ± 20% standard
TCR	± 100ppm/°C

STANDARD ELECTRICAL SPECIFICATIONS	
PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Moisture resistance, MIL-STD-202, Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 12mW	± 0.5% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 1000 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at 150°C)	25mW maximum
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

DIMENSIONS in inches



SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.010 x 0.020 ± 0.002 (0.25 x 0.5 ± 0.08mm)
Chip thickness	0.010 ± 0.002 (0.25 ± 0.05mm)
Chip substrate material	99.6% alumina, 2 - 4 microinch finish
Resistor material	Tantalum nitride, self passivating
Bonding pad size	0.005 x 0.006 (0.12 x 0.24mm)
Number of pads	2
Pad material	25kÅ minimum gold standard
Backing	None

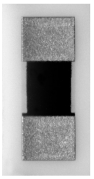
OPTIONS: Terminations: Aluminum
Gold back for solder die attach
Contact Applications Engineer

ORDERING INFORMATION

Example: 100% visualled, 50Ω, ± 10%, ± 100ppm/°C TCR, Gold Pads, Class H visual inspection

W	**MIB**	**002**	**5000**	**B**	**K**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4% AQL)			Use first 4 digits significant digits of the resistance	**B** = 0.01 **A** = 0.1 **0** = 1	**F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10% **M** = 20%

Thin Film Microwave Resistor



Product may not be to scale

The MIC resistor chips on alumina are designed with low shunt capacitance. Most lower value resistor geometrics are compatible with strip lines, making them ideally suited for microwave circuits.
These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The MICs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

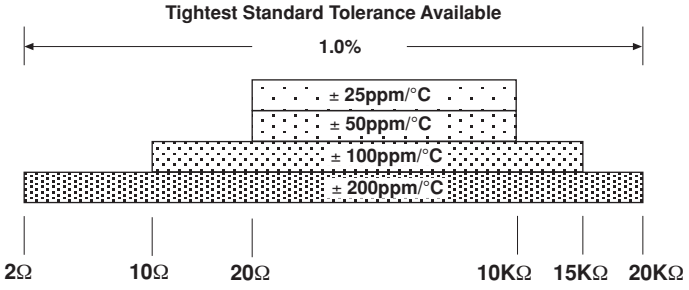
- Small chip size: 0.020 x 0.040 inches
- Microwave resistance range: 20Ω - 1kΩ
- Overall resistance range: 2Ω to 20kΩ
- Alumina substrate
- Low stray capacitance: < 0.2pF
- Resistor material: tantalum nitride, self passivating
- Moisture resistant

APPLICATIONS

Vishay EFI MIC chip resistors provide excellent high-frequency response and are ideally suited for prototyping.
Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE		MICROWAVE	
CLASS H*	CLASS K*	CLASS H*	CLASS K*
004	034	-	-
002	032	-	-
001	031	014	-
003	033	016	017
Gold Termination			

*MIL-PRF-38534 inspection criteria

NOTE: Only 20Ω to 1kΩ are standard strip line designs for Microwave applications

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Moisture resistance, MIL-STD-202, Method 106	± 0.1% maximum ΔR/R
Stability, 1000 hours, + 125°C, 62mW	± 0.2% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.1% maximum ΔR/R
High temperature exposure, + 150°C, 1000 hours	± 0.2% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at 150°C)	125mW maximum
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.1% maximum ΔR/R

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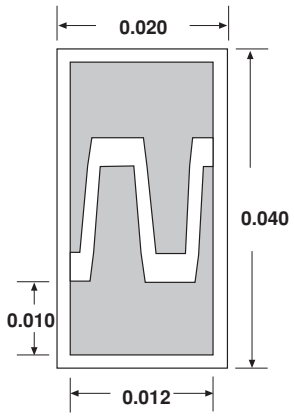
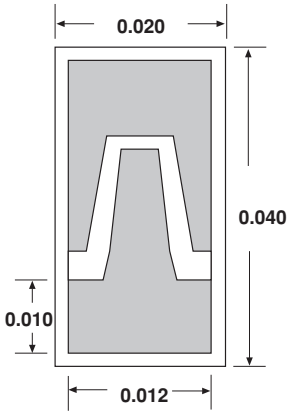
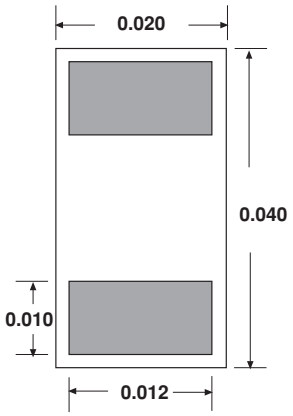
DIMENSIONS in inches



TYPICAL RANGE
2Ω - 6Ω



TYPICAL RANGE
6.2Ω - 19Ω



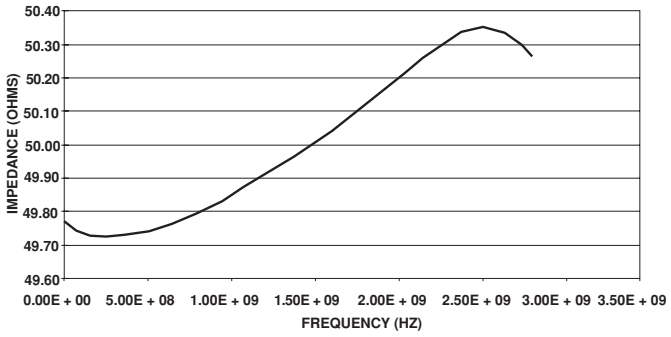
TYPICAL RANGE
20Ω - 20KΩ

SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.020 x 0.040 ± 0.003 (0.5 x 1.0 ± 0.076mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	99.6% alumina, 2 - 4 microinch finish
Resistor material	Tantalum nitride, self passivating
Bonding pad size	0.010 x 0.012 (0.254 x 0.30mm) minimum
Number of pads	2
Pad material	25kÅ minimum gold standard
Backing	None

OPTIONS: Terminations: Aluminum, Nickel solder (62/32/2)
Gold back for solder die attach
Contact Applications Engineer

IMPEDANCE VS FREQUENCY
50Ω, 20 x 40 MIL SIZE

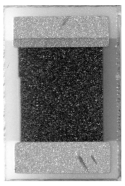


ORDERING INFORMATION

Example: 100% visualled, 50Ω, ± 10%, ± 100ppm/°C TCR, Gold Pads, Class H visual inspection

W	**MIC**	**001**	**5000**	**B**	**K**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4% AQL)			Use first 4 digits significant digits of the resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100	**F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Thin Film Microwave Resistor



Product may not be to scale

The MIF resistor chips on alumina are designed with low shunt capacitance. Resistor geometrics are compatible with strip lines, making them ideally suited for microwave circuits. These chips are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The MIFs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- Small single chip size: 0.016 x 0.020 inches
- Microwave resistance range: 20Ω to 100Ω
- Overall resistance range: 20Ω to 2kΩ
- Alumina substrate
- Low stray capacitance: < 0.2pF
- Resistor material: tantalum nitride, self passivating
- Moisture resistant
- Power: 50mW

APPLICATIONS

Vishay EFI MIF chip resistors provide excellent high frequency response and are ideally suited for prototyping. Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES	
Resistance Range	20Ω to 100Ω
Tolerance	± 1%, ± 5%, ± 10%, ± 20% standard
TCR	± 100ppm/°C

STANDARD ELECTRICAL SPECIFICATIONS	
PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Moisture resistance, MIL-STD-202, Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 25mW	± 0.5% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 1000 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at 150°C)	50mW maximum
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

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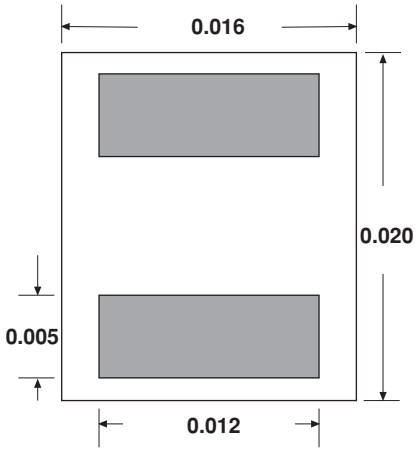
DIMENSIONS in inches



SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.016 x 0.020 ± 0.003 (0.40 x 0.5 ± 0.076mm)
Chip thickness	0.010 ± 0.001 (0.25 ± 0.025mm)
Chip substrate material	99.6% alumina, 2 - 4 microinch finish
Resistor material	Tantalum nitride, self passivating
Bonding pad size	0.005 x 0.012 (0.125 x 0.30mm)
Number of pads	2
Pad material	25kÅ minimum gold standard
Backing	None

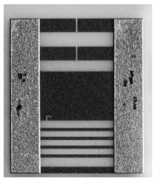
OPTIONS: Terminations: Aluminum/Solder
Gold back for solder die attach
5 mil chip thickness
Contact Applications Engineer

ORDERING INFORMATION

Example: 100% visualled, 50Ω, ± 10%, ± 100ppm/°C TCR, Gold Pads, Class H visual inspection

W	**MIF**	**002**	**5000**	**B**	**K**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4% AQL)			Use first 4 digits significant digits of the resistance	**B** = 0.01 **A** = 0.1 **0** = 1	**F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10% **M** = 20%

Thin Film Microwave Resistor



Product may not be to scale

The MID resistor chips on alumina are designed for low shunt capacitance applications with 200mW power requirements.
These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The MIDs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

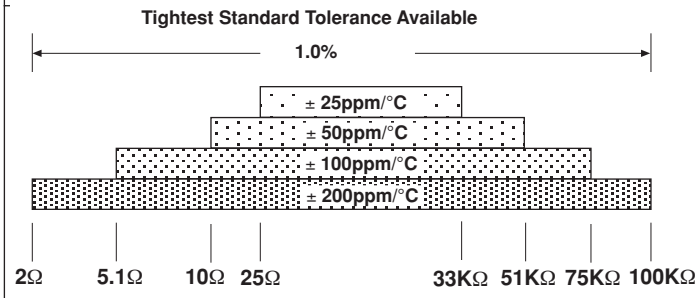
- Chip size: 0.050 inches square
- Microwave resistance range: 18Ω to 500Ω
- Overall resistance range: 2Ω to 100kΩ
- Alumina substrate
- Low stray capacitance: < 0.2pF
- Power: 200mW
- Resistor material: tantalum nitride, self passivating
- Moisture resistant

APPLICATIONS

Vishay EFI MIC chip resistors provide excellent high-frequency response and are ideally suited for prototyping.
Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE		MICROWAVE	
CLASS H*	CLASS K*	CLASS H*	CLASS K*
003	007	-	-
002	006	-	-
001	005	022	-
000	004	008	009

*MIL-PRF-38534 inspection criteria

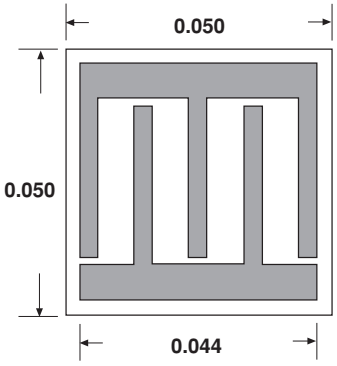
NOTE: Only 18Ω to 500Ω are standard strip line designs for Microwave applications

STANDARD ELECTRICAL SPECIFICATIONS

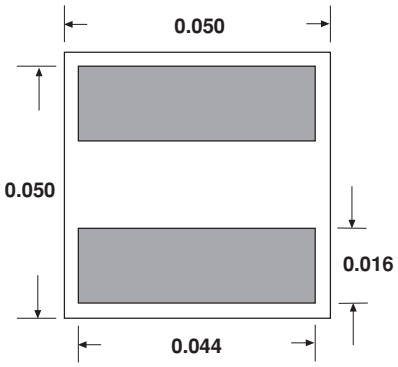
PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Moisture resistance, MIL-STD-202, Method 106	± 0.1% maximum ΔR/R
Stability, 1000 hours, + 125°C, 100mW	± 0.2% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.1% maximum ΔR/R
High temperature exposure, + 150°C, 1000 hours	± 0.2% maximum ΔR/R
Dielectric voltage breakdown	400V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at 150°C)	200mW maximum
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.1% maximum ΔR/R

VISHAY ELECTRO-FILMS • FRANCE +33.4.93.37.28.24 FAX: +33.4.93.37.27.31 • GERMANY +49.9287.710 FAX: +49 9287.70435 • ISRAEL +972.3.557.0945 FAX: +972.3.558.9121
• ITALY + 39.2.300.11911 FAX: +39.2.300.11999 • JAPAN +81.3.5464.6411 FAX: +81.3.5464.6433 • SINGAPORE +65.788.6668 FAX: +65.788.0988
• SWEDEN +46.8.594.70590 FAX: +46.8.594.70581 • UK +44 191 514 8237 FAX: +44 1953 457 722 • USA: (401) 738-9150 FAX: (401) 738-4389

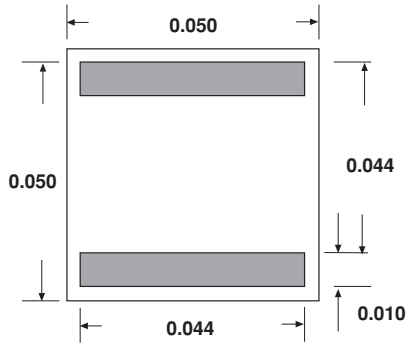
DIMENSIONS in inches



TYPICAL RANGE
2Ω - 7.9Ω



TYPICAL RANGE
8Ω - 17Ω



TYPICAL RANGE
18Ω - 100KΩ

SCHEMATIC

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.050 x 0.050 ± 0.003 (1.27 x 1.27 ± 0.076mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	99.6% alumina, 2 - 4 microinch finish
Resistor material	Tantalum nitride, self passivating
Bonding pad size	0.010 x 0.044 (0.254 x 1.11mm)
Number of pads	2
Pad material	25kÅ minimum gold standard
Backing	None

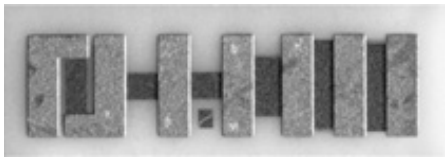
OPTIONS: Terminations: Aluminum, Nickel solder (62/32/2)
Gold back for solder die attach
Contact Applications Engineer

ORDERING INFORMATION

Example: 100% visualled, 50Ω, ± 10%, ± 100ppm/°C TCR, Gold Pads, Class H visual inspection

W	**MID**	**001**	**5000**	**B**	**K**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4% AQL)		See Process Code table	Use first 4 digits significant digits of the resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100	**F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10% **M** = 20% **L** = 25% **N** = 505

Thin Film Tapped Microwave Resistor



Product may not be to scale

The TMR resistor chips on alumina are designed with multiple low ohm taps for circuit trimming. The resistor geometries are compatible with strip lines, making them ideally suited for microwave circuits.
These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The TMRs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- Six resistors on a single chip: size 0.020 x 0.060 inches
- Resistance range: 10Ω to 240Ω
- Alumina substrate
- Low stray capacitance: < 0.2pF
- Resistor material: tantalum nitride self passivating

APPLICATIONS

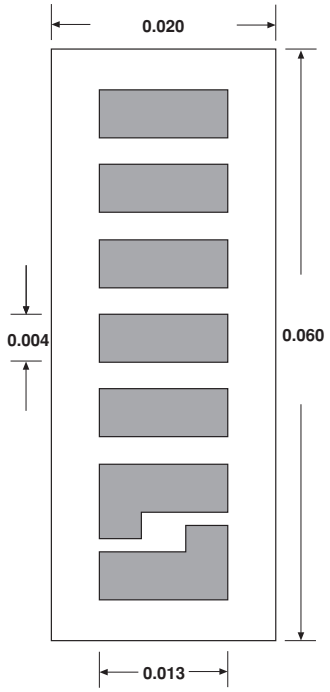
Vishay EFI TMR chip resistors provide excellent high frequency response and are ideally suited for prototyping.
Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters
- Limiters

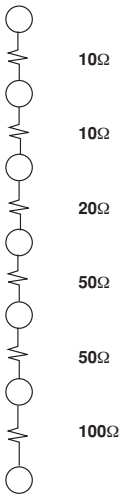
TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES	
Individual resistances	10Ω, 10Ω, 20Ω, 50Ω, 50Ω, 100Ω
Total resistance	240Ω
Tolerance	± 10% of total value
TCR	± 100ppm/°C

STANDARD ELECTRICAL SPECIFICATIONS	
PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
Moisture resistance, MIL-STD-202, Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 62mW	± 1.0% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure, + 150°C, 1000 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at 150°C)	125mW
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

DIMENSIONS in inches



SCHEMATIC



MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip size	0.020 x 0.060 ± 0.003 (1.5 x 0.5 ± 0.08mm)
Chip thickness	0.010 ± 0.002 (0.25 ± 0.05mm)
Chip substrate material	99.6% alumina, 2 - 4 microinch finish
Resistor material	Tantalum nitride, self passivating
Bonding pad size	0.004 x 0.013 (0.10 x 0.33mm)
Number of pads	7
Pad material	15kÅ minimum gold
Backing	None

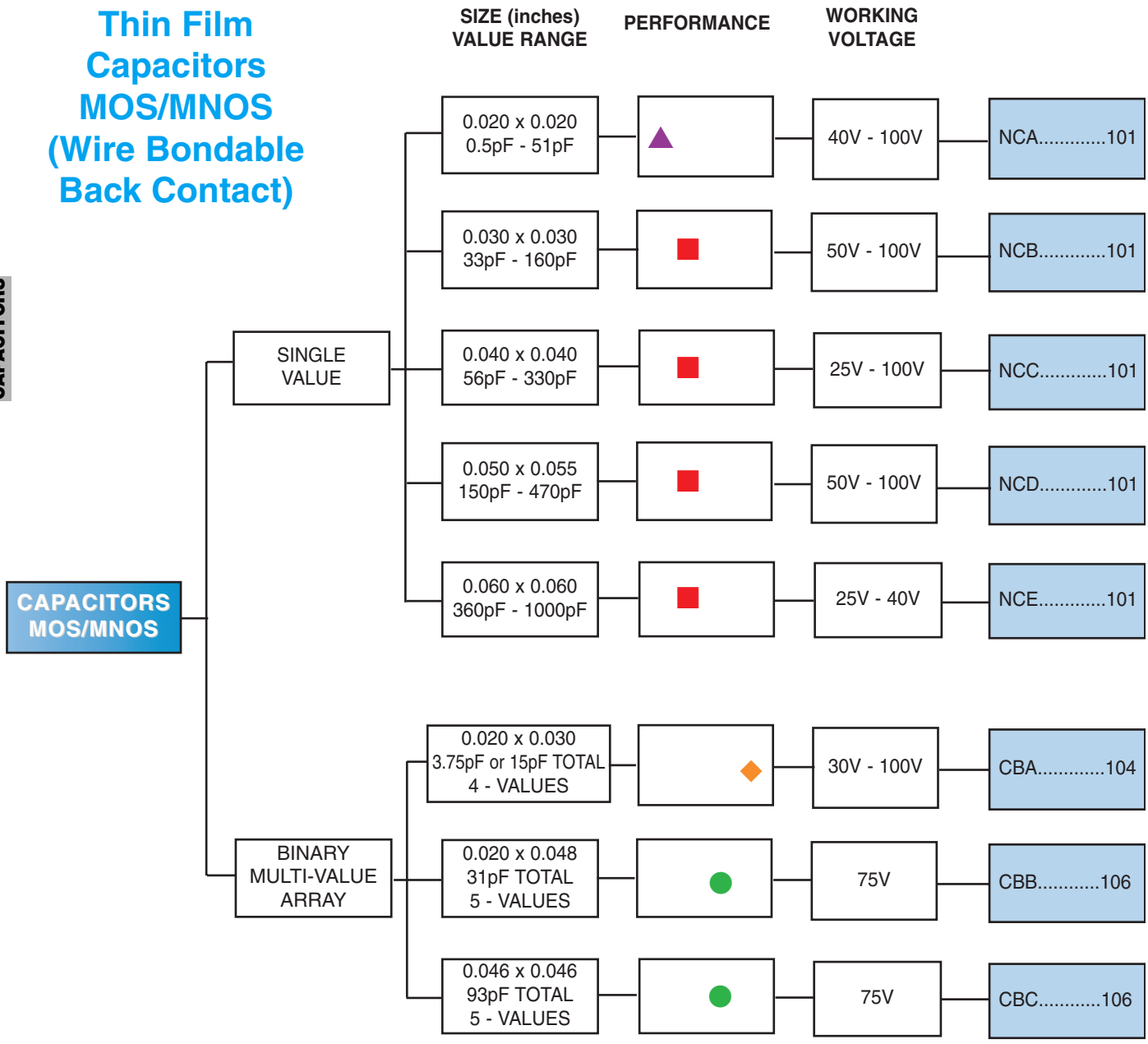
OPTIONS: Gold back for solder die attach
Contact Applications Engineer

ORDERING INFORMATION

Example: 100% visualled, 240Ω, ± 10%, ± 100ppm/°C TCR, Gold Pads, Class H visual inspection

W	TMR	005	2400	A	K
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4% AQL)		See Process Code table	Use first 4 digits significant digits of the resistance (R_T)	**A** = 0.1	**K** = 10% **M** = 20% **L** = 25% **N** = 50%

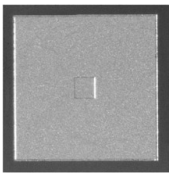
Thin Film Capacitors MOS/MNOS (Wire Bondable Back Contact)



Performance Key

TCC	TOL
▲	+ 15 ± 25ppm/°C / 5%
■	+ 45 ± 25ppm/°C / 5%
●	+ 45 ± 25ppm/°C / 10%
◆	+ 45 ± 25ppm/°C / 25%

Thin Film Single Value Chip and Wire Capacitors



Product may not be to scale

The NC series of thin film capacitors has the advantage of increased performance and smaller size when compared with its thick film counterparts. These chips are available in sizes down to 20 mil square and in capacitances up to 1000pF.

Parts require epoxy or eutectic die attach to substrate and one wire bond.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The NC's are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

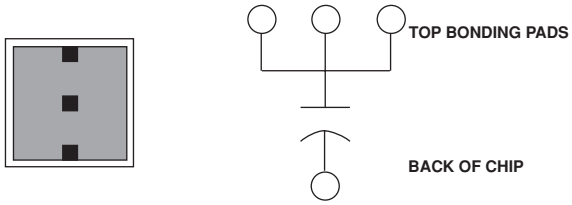
- Small size: 0.020 to 0.060 inches square
- Substrate: silicon with gold backing
- Dielectric: silicon dioxide/silicon nitride
- Capacitance range: 0.5pF to 1000pF

APPLICATIONS

The NC series of capacitor chips are designed for assembly in hybrid circuits using conventional wire-bonding techniques. They provide excellent stability and performance, and their small size gives the hybrid designer greater layout flexibility. They are available as MNOS or MOS capacitors. The MOS version is to be preferred when low dielectric absorption is required.

ELECTRICAL SCHEMATIC NCA/NCB/NCC

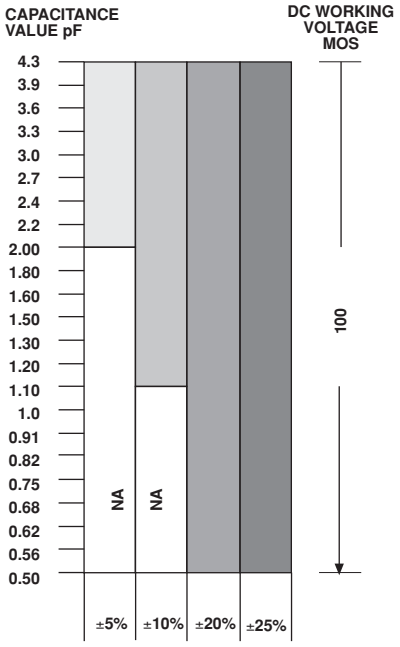
ELECTRICAL SCHEMATIC NCD/NCE

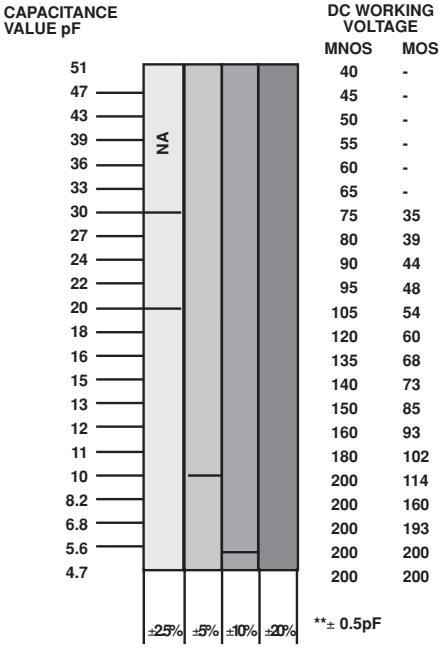


STANDARD ELECTRICAL SPECIFICATIONS	
PARAMETER	
Peak voltage at + 25°C	1.5 x working voltage
Dissipation factor, 1kHz, $1V_{rms}$, + 25°C	0.05% MNOS 0.1% MOS
Q at 1mHz, $50mV_{rms}$, + 25°C	1000 minimum
TCC, - 55°C to + 150°C	+ 45 ± 25ppm/°C MNOS + 15 ± 25ppm/°C MOS
Insulation resistance at working voltage, + 25°C	10^9 minimum
Operating temperature range	- 55°C to + 125°C
Thermal shock	± 0.25% + 0.25pF maximum ΔC/C
Moisture resistance, MIL-STD-202, Method 106	± 1.0% + 0.25pF maximum ΔC/C
Short time overload, + 25°C, 5 seconds, 1.5 x working voltage	± 0.25% + 0.25pF maximum
High temperature exposure, 100 hours at 150°C ambient	± 0.25% + 0.25pF maximum ΔC/C
Life, MIL-STD-202, Method 108 Condition D, + 125°C ambient, 100 hours at working voltage	± 0.25% + 0.25pF maximum ΔC/C

DC WORKING VOLTAGES VALUES AND TOLERANCES

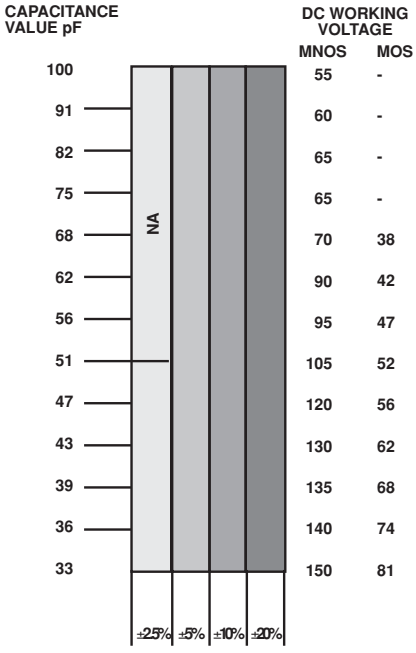
NCA 0.020 Inches Square



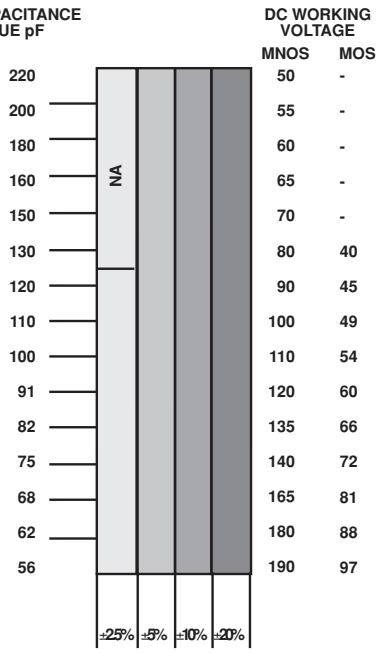


NA = NOT AVAILABLE

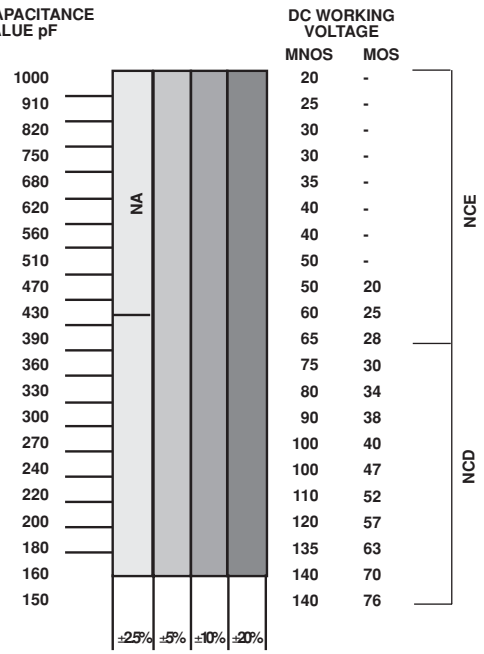
NCB 0.030 inches square



NCC 0.040 inches square



NCD 0.055 inches square
NCE 0.060 inches square



DIMENSIONS

0.5pF - 1.3pF | **1.4pF - 3.9pF** | **4pF - 9.1pF** | **10pF - 51pF**

NCA
0.020 ± 0.003 inches square

33pF - 100pF | **56pF - 220pF** | **150pF - 510pF** | **360pF - 1000pF**

NCB
0.030 ± 0.003 inches square

NCC
0.040 ± 0.003 inches square

NCD
0.055 ± 0.003 inches square

NCE
0.060 ± 0.003 inches square

MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip size	Per Diagrams
Chip thickness	0.010 ± 0.002 (0.25 ± 0.05mm)
Chip substrate material	Semiconductor silicon
Dielectric	Silicon dioxide/Silicon nitride
Bond pad	0.005 x 0.005 minimum, 10kÅ aluminum
Backing	3kÅ minimum gold

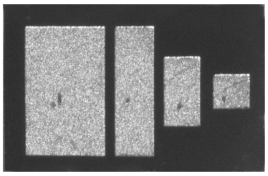
OPTIONS: Gold bond pads 15kÅ
Lower profile version is available, Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visualled, 2pF, ± 5%, 20 mil MOS capacitor, Aluminum Pads, Class H visual inspection

W	**NCA**	**017**	**2000**	**C**	**J**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	CAPACITANCE VALUE (pF)	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix trays per MIL-STD-883 **X** = Sample, commercial visually inspected loaded in matrix trays (4% AQL)	NCA NCB NCC NCD NCE	**017** = MOS Aluminum **000** = MNOS Aluminum	Use first 4 digits significant digits of capacitance	**C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1	**D** = ± 0.5pF **H** = ± 2.5%* **J** = ± 5.0% **K** = ± 10% **M** = ± 20% **L** = ± 25% **N** = ± 50% * MOS only

Thin Film Binary MOS Capacitors



Product may not be to scale

The CBA MOS capacitor chips each contain four different capacitors in binary increments allowing the user many choices in value selection. Two versions of CBA capacitors are available: one with a total capacitance of 3.75pF and one with a total capacitance of 15pF.
These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The CBAs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- User value selection
- Four capacitors with common connection
- Capacitance range: 0.25pF to 15pF in binary increments
- Dielectric: silicon dioxide
- Chip size: 0.019 x 0.030 inches
- Substrate: silicon with gold backing

APPLICATIONS

Vishay EFI CBA binary MOS multi-value capacitor chips are designed for hybrid packages in which microwave circuits are to be trimmed. This is done on the CBA chips by selecting the bonding pad for the required capacitance and wire-bonding by conventional techniques.

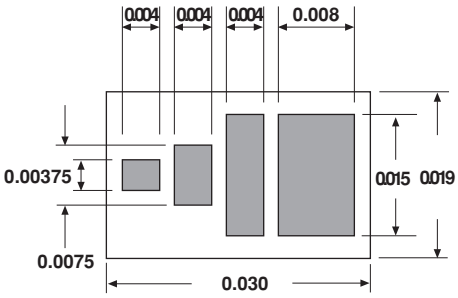
WV (DC) VALUES AND TOLERANCES

CAPACITOR MODEL	CBA 3.75pF	CBA 15pF
Total capacitance	3.75pF	15pF
Individual capacitance	0.25pF, 0.50pF, 1.0pF, 2.0pF	1.0pF, 2.0pF, 4.0pF, 8.0pF
Tolerance	± 25%	± 10%
DC Working voltage	100V	30V

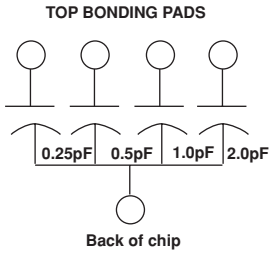
STANDARD ELECTRICAL SPECIFICATIONS

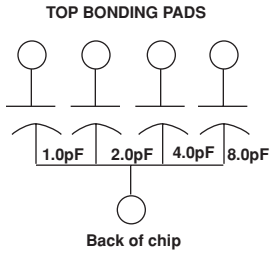
PARAMETER	
Peak voltage at + 25°C	1.5 x working voltage
Dissipation factor, 1kHz, 1V_{rms}, + 25°C	0.1% maximum MOS
Q at 1mHz, 50mV_{rms}, + 25°C	1000 minimum
TCC, - 55°C to + 150°C	+ 15 ± 25ppm/°C
Insulation resistance at working voltage, + 25°C	10^9 minimum
Operating temperature range	- 55°C to + 150°C
Thermal shock	± 0.25% + 0.25pF maximum ΔC/C
Moisture resistance, MIL-STD-202, Method 106	± 1.0% + 0.25pF maximum ΔC/C
Short time overload, + 25°C, 5 seconds; 1.5 x working voltage	± 0.25% + 0.25pF maximum ΔC/C
High temperature exposure: 100 hours at + 150°C ambient	± 0.25% + 0.25pF maximum
Life, MIL-STD-202, Method 108, Condition D, + 125°C ambient, 1000 hours at working voltage	± 2.0% + 0.25pF maximum ΔC/C

CONFIGURATIONS in inches



SCHEMATIC





MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.019 x 0.030 ± 0.002 (0.48 x 0.75 ± 0.05mm)
Chip thickness	0.010 ± 0.003 (0.25 ± 0.08mm)
Chip substrate material	Semiconductor Silicon
Dielectric	Silicon dioxide (MOS)
Bonding pads	10kÅ minimum aluminum
Backing	3kÅ minimum gold

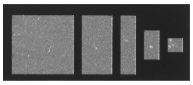
OPTIONS: Gold bonding pads 15 kÅ minimum
Other value combinations available
Consult Applications Engineer

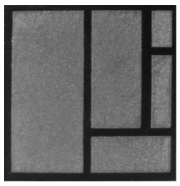
ORDERING INFORMATION

Example: 100% visualled, 3.75pF ± 25%, Aluminum Pads, Class H visual inspection

W	**CBA**	**004**	**3750**	**C**	**L**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	CAPACITANCE VALUE (pF)	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4% AQL)		**004** = CBA	Use first 4 significant digits of the capacitance (C_T)	**C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10	**K** = 10% **M** = 20% **L** = 25% **N** = 50%

Thin Film Binary MOS Capacitors





Product may not be to scale

The CBB and CBC MOS capacitor chips each contain five different capacitors in binary increments allowing the user many choices in value selection.
These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The CBB and CBCs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- User value selection
- Five capacitors on a 0.019 x 0.048 inches (CBB) or 0.044 inches square (CBC) chip
- Capacitance range: 1.0pF to 93pF in binary increments
- Dielectric: silicon dioxide
- Low dielectric loss
- Substrate: silicon with gold backing

APPLICATIONS

Vishay EFI CBB and CBC binary MOS multi-value capacitor chips are designed to be a useful device for trimming hybrid circuits by adding or subtracting capacitance, using normal wire-bonding techniques.

WV (DC) VALUES AND TOLERANCES

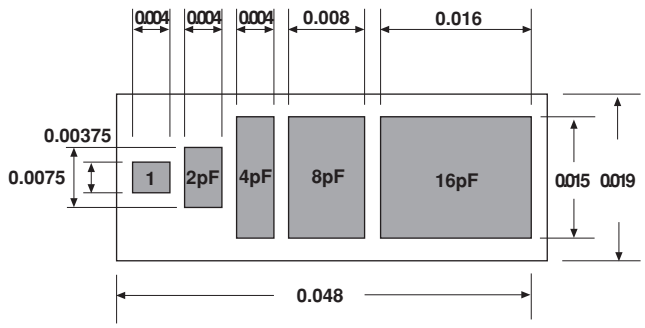
CAPACITOR MODEL	CBB	CBC
Total capacitance	31pF	93pF
Individual capacitance	1pF, 2pF, 4pF, 8pF, 16pF	3pF, 6pF, 12pF, 24pF, 48pF
Tolerance	± 10%	± 10%
DC Working voltage	75V	75V

STANDARD ELECTRICAL SPECIFICATIONS

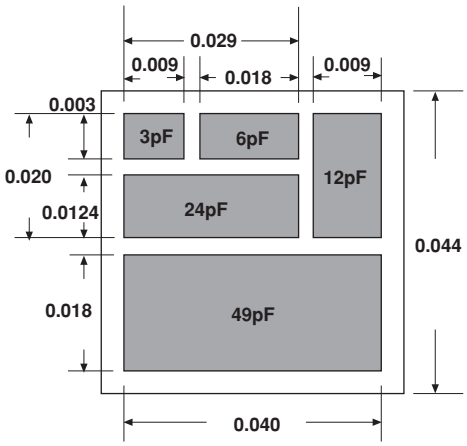
PARAMETER	
Peak voltage at + 25°C	1.5 x working voltage
Dissipation factor, 1kHz, 1V_{rms}, + 25°C	0.1%
Q at 1mHz, 50mV_{rms}, + 25°C	1000 minimum
TCC, - 55°C to + 150°C	+ 15 ± 25ppm/°C
Insulation resistance at working voltage, + 25°C	10^9 minimum
Operating temperature range	- 55°C to + 150°C
Thermal shock	± 0.25% + 0.25pF maximum ΔC/C
Moisture resistance, MIL-STD-202, Method 106	± 1.0% + 0.25pF maximum ΔC/C
Short time overload, + 25°C, 5 seconds; 1.5 x working voltage	± 0.25% + 0.25pF maximum ΔC/C
High temperature exposure: 100 hours at + 150°C ambient	± 0.25% + 0.25pF maximum
Life, MIL-STD-202, Method 108, Condition D, + 125°C ambient, 1000 hours at working voltage	± 2.0% + 0.25pF maximum ΔC/C

CONFIGURATIONS in inches

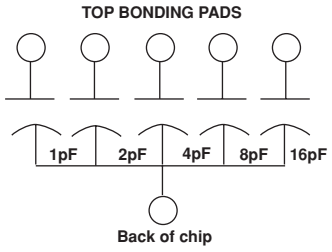
CBB

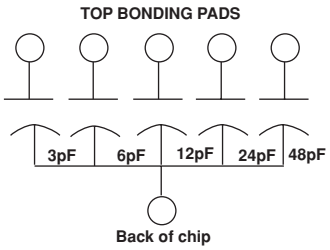


CBC



SCHEMATIC





MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size, CBB CBC	0.019 x 0.048 ± 0.002 (0.48 x 1.2 ± 0.05mm) 0.044 x 0.044 ± 0.002 (1.1 x 1.1 ± 0.05mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Semiconductor Silicon
Dielectric	Silicon dioxide (MOS)
Bonding pads	10kÅ minimum aluminum
Backing	3kÅ minimum gold

OPTIONS: Gold bonding pads 15 kÅ minimum
Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visualled, 93pF, 10%, CBC Capacitor, Aluminum Pads, Class H visual inspection

W	**CBC**	**012**	**9300**	**B**	**K**
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	CAPACITANCE VALUE (pF)	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4% AQL)	CBB CBC	**008** = CBB **012** = CBC	Use first 4 significant digits of the capacitance (C_T)	**C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1	**J** = 5.0% **K** = 10% **M** = 20% **L** = 25% **N** = 50%

Thin Film Filter Network Resistor-Capacitor Array (Wire Bondable)

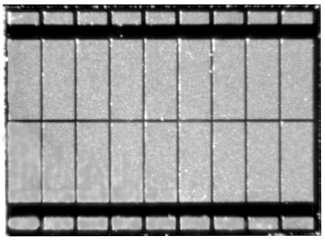
THIN FILM FILTER NETWORK RESISTOR/CAPACITOR ARRAY	MULTI-VALUE	SIZE (inches) R - RANGE C - RANGE: 0.125 x 0.135 25, 50 ohms 50, 100, 200, 400pF	PERFORMANCE: ▲	MODEL: RCN.....109

Performance Key

▲

TCR	± 100ppm/°C
TOL	± 10%
TCC	± 200ppm/°C
TOL	± 10%

Thin Film Filter Networks



Product may not be to scale

The RCN series combines resistor and capacitor technology on a single chip to provide filtering capability together with excellent stability. Specifications below are standard but may be changed and customized for the application and are available in widebody SOIC or DIP packages.

These chips are manufactured using Vishay (EFI) sophisticated Thin Film equipment and manufacturing technology. The RCNs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- Standard Resistance range: 25Ω and 50Ω
- Standard Capacitance range: 50pF, 100pF, 200pF, 400pF
- Resistance Tolerance to 1%
  Capacitance Tolerance to 5%
- Capacitor MOS/MNOS
- Resistor material: Tantalum nitride, self-passivating
- Oxidized silicon substrate

APPLICATIONS

The RCN filter chips are used for low pass filters, RFI & EMI, CMOS digital filters, ECL terminators and power supply filters. Contact our Sales Department for any special configurations or requirements that are needed.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND COMBOS (Standard)

Absolute TCR = ± 100ppm/°C
Absolute TCC = + 45 ± 75ppm/°C

R	C	R	C
25Ω	50pF	50Ω	50pF
25Ω	100pF	50Ω	100pF
25Ω	200pF	50Ω	200pF
25Ω	400pF	50Ω	400pF

STANDARD ELECTRICAL SPECIFICATIONS	
PARAMETER	
Noise, MIL-STD-202, Method 308 100Ω - 250kΩ < 100Ω or > 251kΩ	- 35dB typical - 20dB typical
Moisture resistance, MIL-STD-202 Method 106	± 0.5% maximum ΔR/R
Stability, 100 hours, + 125°C 50mW/Res @ WVDC	± 0.5% maximum ΔR/R ± 2.0% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	± 0.1% maximum ΔR/R
High temperature exposure, + 150°C, 1000 hours	± 0.2% maximum ΔR/R
Insulation resistance	10^9 minimum
Operating voltage	25V maximum
DC power rating at - 55°C to + 125°C (100V maximum)	50mW
5 x rated power short-time overload, + 25°C, 5 seconds (100V maximum)	± 0.5% maximum ΔR/R

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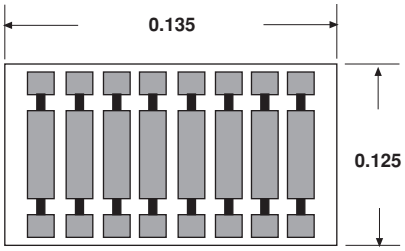
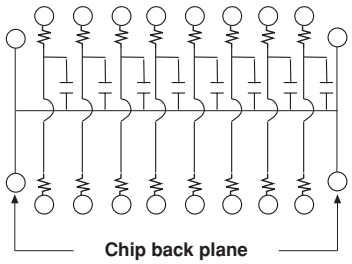
DIMENSIONS in inches



SCHEMATIC



MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.135 x 0.125 ± 0.005 (3.429 x 3.175 ± 0.127mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pad size	0.005 x 0.007 (0.127 x 0.178mm)
Number of pads	16 (8 x RC)
Pad material	10kÅ minimum aluminum
Backing	3kÅ minimum Gold

OPTIONS: Gold bonding pads 15kÅ minimum thickness
Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visualled, 25Ω, ± 20%, 200pF ± 20%, ± 100ppm/°C, Aluminum Pads, Class H visual inspection

P/N:	**W**	**RCN**	**200**	**250**	**A**	**201**	**M**
	INSPECTION /PACKAGING	PRODUCT FAMILY	SERIES	RESISTANCE VALUE	RESISTOR TOLERANCE	CAPACITOR VALUE	CAPACITANCE TOLERANCE
	W = 100% visually inspected parts in matrix trays per MIL-STD-883 **X** = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)			Use the first 3 significant digits of the resistance & multiplier	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100	Use the first 3 significant digits of the capacitance & multiplier	**J** = 5.0% **K** = 10% **M** = 20% **N** = 25%

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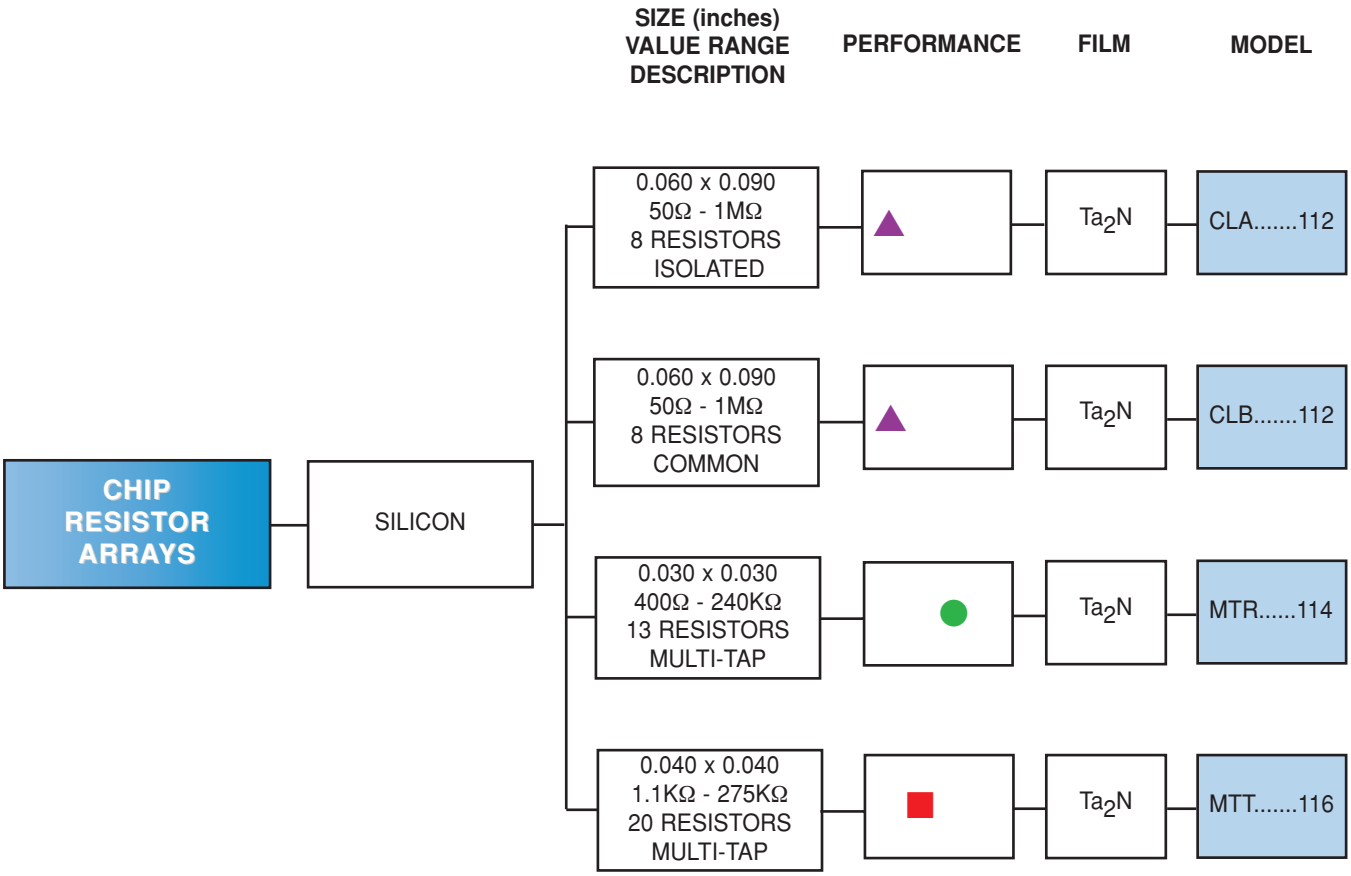
Thin Film
Chip Resistor Arrays
Wire Bondable



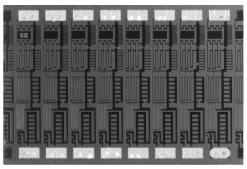
Performance Key

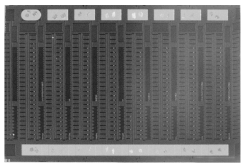
▲	
TCR	± 10ppm/°C
TOL	± 0.1%

■	
TCR	± 250ppm/°C
TOL	1%

●	
TCR	± 100ppm/°C
TOL	10%

Thin Film Eight Resistor Array





Product may not be to scale

The CLA and CLB resistor arrays are the hybrid equivalent to the eight resistor common connection and isolated networks available in sips or dips. The resistors are spaced on 0.010 inches centers resulting in minimal space requirements.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The CLA and CLBs are 100% electrically tested and visually inspected to MIL-STD-883.

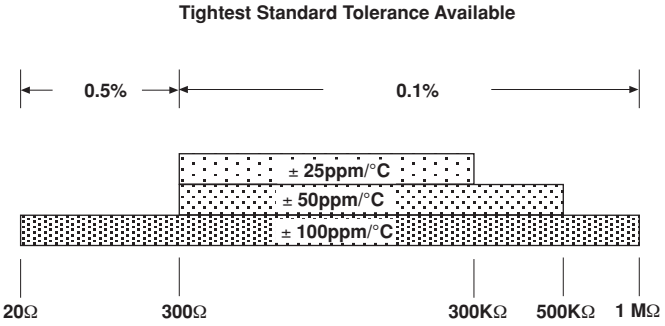
FEATURES

- Eight equal value resistors on a 0.060 x 0.090 inch chip
- Resistance range: 20Ω to 1MΩ
- Excellent TCR tracking
- Resistor material: tantalum nitride, self-passivating
- Oxidized silicon substrate for good power dissipation
- Custom values available
- Moisture resistant

APPLICATIONS

The CLA and CLB thin film resistor arrays are designed for hybrid packages requiring up to eight resistors of the same resistance value and tolerance, as well as excellent TCR tracking. For such hybrids, they afford great savings in cost and space.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
026	054
017	049
008	045

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
TCR tracking spread	± 5ppm/°C
Noise, MIL-STD-202, Method 308 100Ω - 250kΩ < 100Ω or > 251kΩ	 - 35dB typical - 20dB typical
Moisture resistance, MIL-STD-202, Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 25mW Absolute Ratio	 ± 0.25% maximum ΔR/R ± 0.05% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202 Method 107, Test condition F	± 0.1% maximum ΔR/R
High temperature exposure ± 150°C, 100 hours	± 0.2% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V
DC power rating at + 70°C, (derated to zero at 175°C)	50mW per resistor
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.1% maximum ΔR/R

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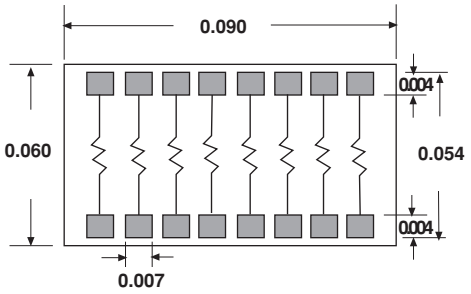
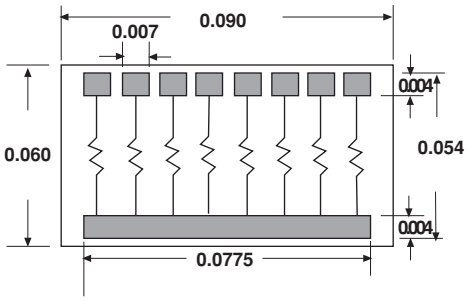
DIMENSIONS in inches

CLA



CLB



MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip size	0.060 x 0.090 ± 0.002 (1.50 x 2.26 ± 0.05mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pads	0.004 x 0.007 (0.10 x 0.178mm)
Number of top pads	CLA - 16 CLB - 9
Pad material	10kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

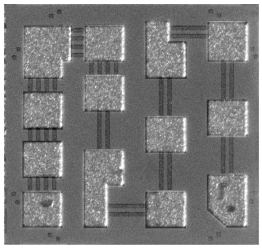
OPTIONS: Gold backing for eutectic die attach
For custom configurations, Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visualled, 10kΩ, ± 1%, ± 100ppm/°C TCR, CLA Format, Aluminum Pads, Class H visual inspection

P/N:	W	CLA	008	1000	1	F
	INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
	W = 100% visually inspected parts per MIL-STD-883 in matrix trays **X** = Sample, visually inspected loaded in matrix trays (4% AQL)		See Process Code table	Use first 4 significant digits of the resistance	**D** = 0.0001 **C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000 **4** = 10000	**B** = 0.1% **C** = 0.2% **D** = 0.5% **F** = 1.0% **G** = 2.0% **H** = 2.5% **J** = 5.0% **K** = 10%

Thin Film Multi-Tap Resistors



Product may not be to scale

FEATURES

- Selectable values by wire bonding
- Chip size: 0.030 inches square
- Standard resistance range: 100Ω to 24kΩ or 800Ω to 240kΩ
- Resistor material: Tantalum nitride, self-passivating
- Oxidized silicon substrate for good power dissipation
- Ideally suited for hybrid prototyping

The MTR multi-tap resistors, available in two formats, offer eleven taps allowing the user to select specified increments a wide range of values. The desired resistance value is obtained by bonding the wires to the appropriate pads.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The MTRs are 100% electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

The MTR series of multi-tap resistor chips are designed to satisfy the requirements of prototype development and circuit trimming in hybrid packages through selective wire-bonding.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES

			PROCESS CODE	
			CLASS H*	CLASS K*
Total resistance range	Format A	100Ω, 200Ω, 400Ω, 800Ω, 2.4kΩ, 8kΩ, 24kΩ	050	060
	Format B	800Ω, 2.4kΩ, 8kΩ, 24kΩ, 80kΩ, 160kΩ, 240kΩ	051	061
7 resistors between Pads 1 and 8 5 resistors between Pads 8 and 13		Each 12.5% of total resistance Each 2.5% of total resistance		
Standard tolerances		± 10%, ± 20% of total resistance of all 12 resistors		
TCR		± 100ppm/°C		

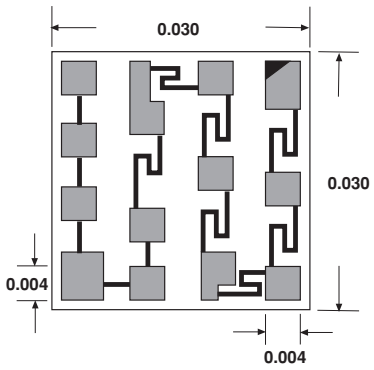
EXAMPLE: When the total resistance value is 8kΩ, the resistors between pads 8 and 13 are 200 each, and the resistors between Pads 1 and 8 are 1k each.

*MIL-PRF-38534 inspection criteria

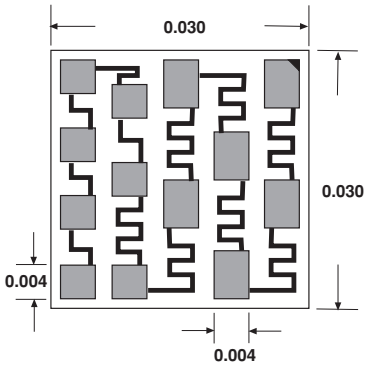
STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
TCR tracking between elements	± 5ppm/°C
Noise, MIL-STD-202, Method 308	- 30dB typical
Moisture resistance, MIL-STD-202, Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 125mW	± 0.5% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202 Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure + 150°C, 100 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C, (derated to zero at + 175°C)	250mW, total R
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

DIMENSIONS in inches

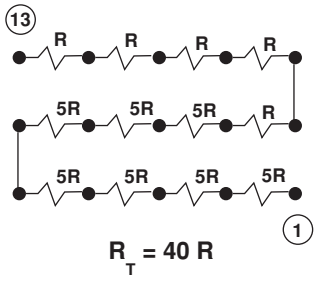


Format A



Format B

SCHEMATIC



R_T = 40 R

CHIP RESISTOR ARRAYS

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.030 x 0.030 ± 0.003 (0.762 x 0.762 ± 0.076mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pads	0.004 x 0.004 (0.10 x 0.10mm)
Number of top pads	13
Pad material	10kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

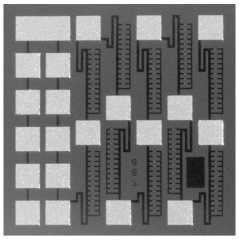
OPTIONS: Gold back for eutectic die attach
Gold bonding pads 15kÅ minimum thickness
Other values available on request, Consult Application Engineer

ORDERING INFORMATION

Example: 100% visualled, 8kΩ, ± 10%, ± 100ppm/°C TCR, Alumimun Pads, Format B, Class H visual inspection

P/N:	W	MTR	051	8000	0	K
	INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
	W = 100% visually inspected parts in matrix trays per MIL-STD-883 **X** = Sample, commercial visually inspected parts in matrix trays (4% AQL)		**050** = Format A **051** = Format B See Process Code table	Use first 4 significant digits of the resistance (R_T)	**A** = 0.1 **0** = 1 **1** = 10 **2** = 100	**K** = 10% **M** = 20% **L** = 25% **N** = 50%

Thin Film Multi-Tap Resistors



Product may not be to scale

FEATURES

- Selectable values by wire bonding
- Resistance range: 1.1kΩ to 275kΩ
- Chip size: 0.038 inches square
- Resistor material tantalum nitride, self-passivating
- Oxidized silicon substrate for good power dissipation
- Ideally suited for hybrid prototyping

The MTT multi-tap resistors offer nineteen taps allowing the user to select specified increments and a wide range of values. The desired resistance value is obtained by bonding the wires to the appropriate pads.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The MTT's are 100% electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

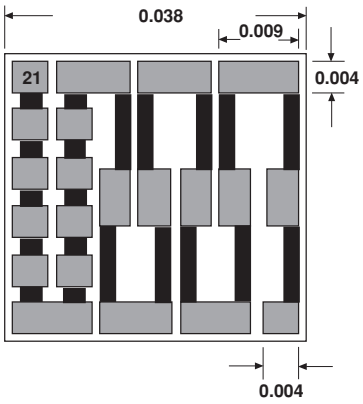
The MTT series of multi-tap resistor chips are designed to satisfy the requirements of prototype development and circuit trimming in hybrid packages through selective wire-bonding.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES	
Total resistance range	1.1kΩ, 2.75kΩ, 5.5kΩ, 11kΩ, 27.5kΩ, 55kΩ, 110kΩ, 275kΩ
10 resistors between Pads 1 and 11 10 resistors between Pads 11 and 21	Each 9.1% of total resistance Each 0.91% of total resistance
Standard tolerances	± 1%, ± 5%, ± 10%, ± 20% of total resistance of all 20 resistors
TCR	± 250ppm/°C

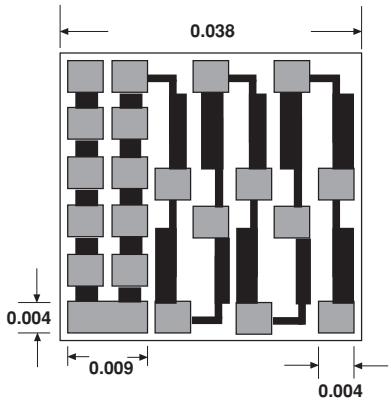
EXAMPLE: When the total resistance value is 55kΩ, the resistors between pads 11 and 21 are 500Ω each, and the resistors between Pads 1 and 11 are 5kΩ each.

STANDARD ELECTRICAL SPECIFICATIONS	
PARAMETER	
TCR tracking between elements	± 5ppm/°C
Noise, MIL-STD-202, Method 308	- 30dB typical
Moisture resistance, MIL-STD-202, Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 125mW	± 0.5% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202 Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure ± 150°C, 100 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C, (derated to zero at + 175°C)	250mW, total R
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

DIMENSIONS in inches

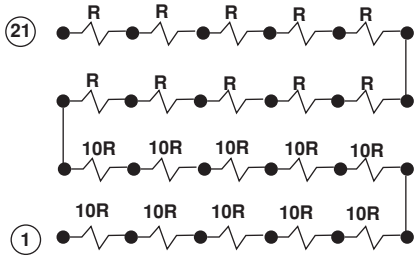


TYPICAL RANGE
1.0kΩ - 5.5kΩ



TYPICAL RANGE
11kΩ - 275kΩ

SCHEMATIC



R_T = 110R

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.038 x 0.038 ± 0.002 (0.762 x 0.762mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pads	0.004 x 0.004 (0.10 x 0.10mm)
Number of pads	21
Pad material	10kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

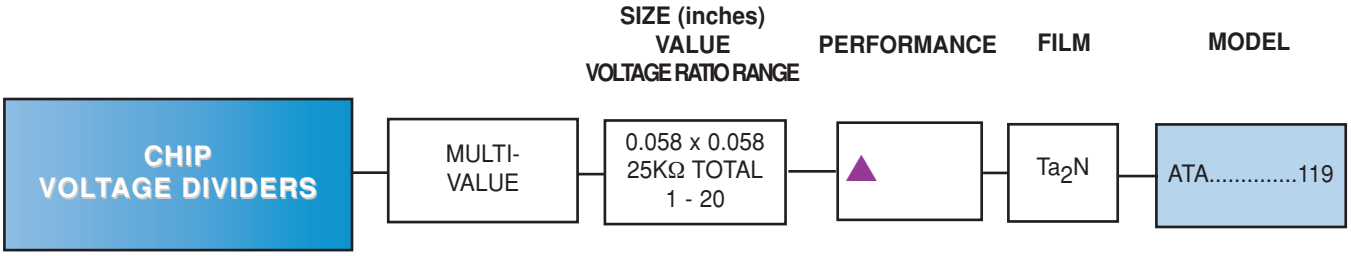
OPTIONS: Gold back for eutectic die attach
Gold bonding pads 15kÅ minimum thickness
Other values available on request, Consult Application Engineer

ORDERING INFORMATION

Example: 100% visualled, 55kΩ, ± 10%, ± 250ppm/°C TCR, Aluminum Pads, Class H visual inspection

P/N:	W	MTT	002	5500	1	K
	INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
	W = 100% visually inspected parts in matrix trays per MIL-STD-883 **X** = Sample, commercial visually inspected parts in matrix trays (4% AQL)		002 = Class H 008 = Class K See Process Code table	Use first 4 significant digits of the resistance (R_T)	**A** = 0.1 **0** = 1 **1** = 10 **2** = 100	**K** = 10% **M** = 20% **L** = 25% **N** = 50%

Thin Film
Chip
Voltage Dividers

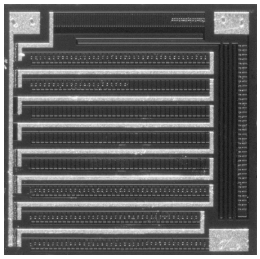


Performance Key

▲

TCR	± 50ppm/°C
TOL	± 5%

Thin Film Voltage Divider Resistors



Product may not be to scale

FEATURES

- Variable ratios
- Chip size: 0.058 inch square
- Resistor material: tantalum nitride, self-passivating
- Oxidized silicon substrate for good power dissipation
- Moisture resistant

The ATA voltage divider is a versatile two-resistor tapped chip whose R_A/R_B ratio can be specified within the values of 1:1 to 20:1.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The ATAs are 100% electrically tested and visually inspected to MIL-STD-883.

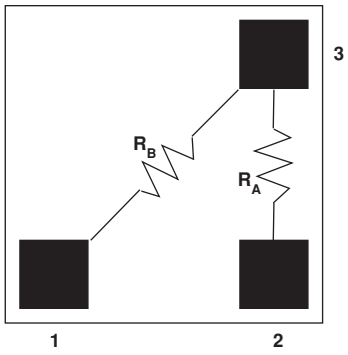
APPLICATIONS

Vishay EFI ATA voltage divider resistor-ratio chips are designed for the tight ratio tolerances generally required in amplifier feedback circuits. The great range of ratio choices makes them specially suitable for this application.

TEMPERATURE COEFFICIENT OF RESISTANCE VALUES AND TOLERANCES	
Resistance ($R_A + R_B$)	25kΩ
Tolerances ($R_A + R_B$)	± 5%
Greatest ratio (R_A/R_B)	20:1
TCR	± 50ppm/°C

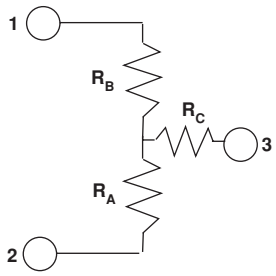
STANDARD ELECTRICAL SPECIFICATIONS	
PARAMETER	
TCR tracking between RA and RB	± 5ppm/°C
Noise, MIL-STD-202, Method 308	- 35dB typical
Moisture resistance, MIL-STD-202, Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 25mW	± 0.25% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202 Method 107, Test condition F	± 0.1% maximum ΔR/R
High temperature exposure + 150°C, 100 hours	± 0.2% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C, (derated to zero at + 175°C)	50mW per resistor
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.1% maximum ΔR/R

CONFIGURATIONS



Shaded areas represent bonding pads.

$$\text{ATTENUATOR FACTOR} = \frac{R_A}{R_A + R_B}$$



Any ratio R_A/R_B from 1 to 20 is available to ± 0.05%
Rc is a parasitic resistor approximately 5Ω in value, which does not effect the performance of the device when it is used into a high impedence load.

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.058 x 0.058 ± 0.003 (1.47 x 1.47 ± 0.076mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pads	0.005 x 0.005 (0.127 x 0.127mm)
Number of top pads	3
Pad material	10kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

OPTIONS: Gold back for eutectic die attach
Contact Applications Engineer

CHIP VOLTAGE DIVIDERS

ATTENUATION TABLE

PART # ATA	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20	**RATIO ACCURACY**	**TEMPERATURE TRACKING**
RATIO R_A/R_B	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20	± 0.05%	± 5ppm/°C maximum ± 2ppm/°C typical
ATTENUATOR FACTOR $R_B/R_A + R_B$	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21	± 0.025% to ± 0.048%	± 2.5ppm/°C to ± 4.8ppm/°C maximum ± 1ppm/°C to ± 2ppm/°C typical
ATTENUATOR FACTOR $R_A/R_A + R_B$	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21	± 0.025% to ± 0.0025%	± 2.5ppm/°C to ± 0.25ppm/°C maximum ± 1ppm/°C to ± 0.15ppm/°C typical

ORDERING INFORMATION

Example: 100% visualled, 25kΩ, ± 5%, ± 100ppm/°C TCR, Ratio = 19.0, Aluminum Pads, Class H visual inspection

P/N:	**W**	**ATA**	**003**	**1900**	**B**	**J**
	INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RATIO VALUE	MULTIPLIER CODE	TOLERANCE CODE
	W = 100% visually inspected parts per MIL-STD-883 **X** = Sample, visually inspected loaded in matrix trays (4% AQL)		003 = Class H 005 = Class K	Use first 4 significant digits of the ratio R_A/R_B - Any ratio between 1 to 20	**C** = 0.001 **B** = 0.01	**J** = 5.0%

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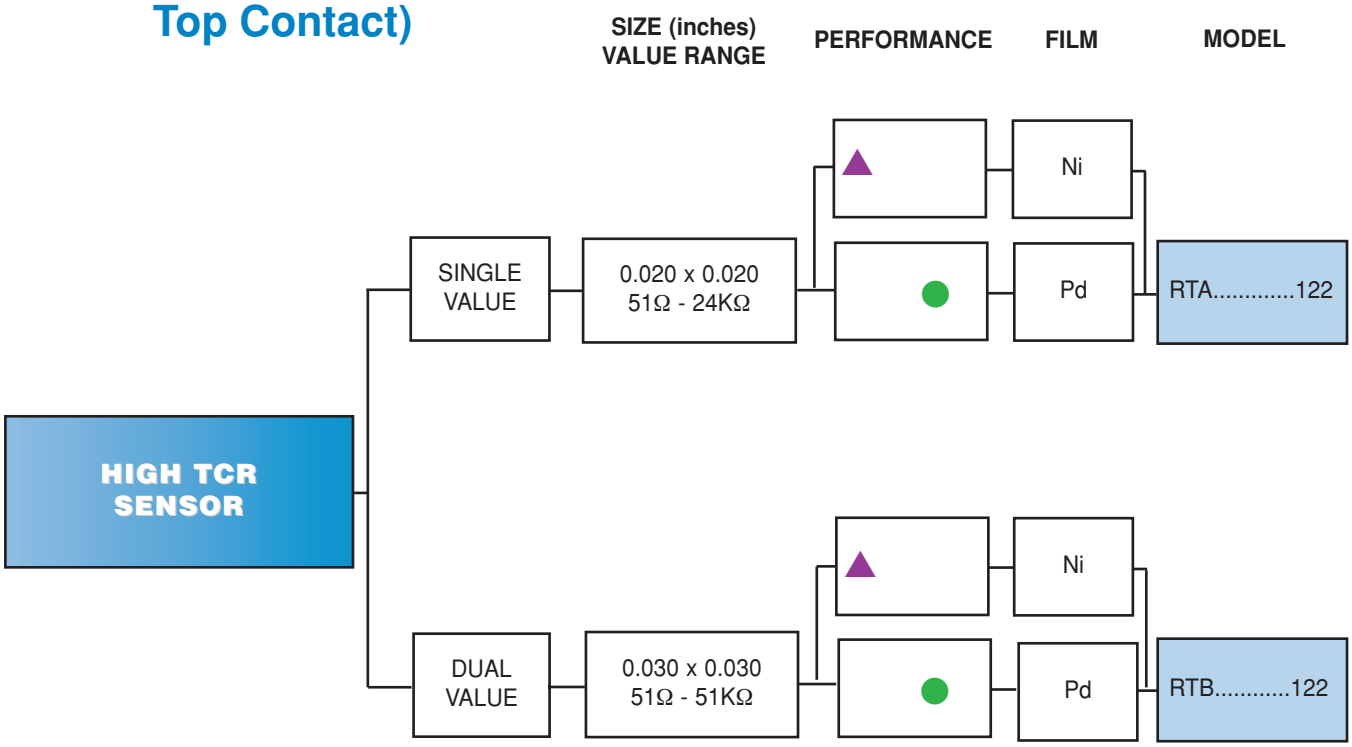
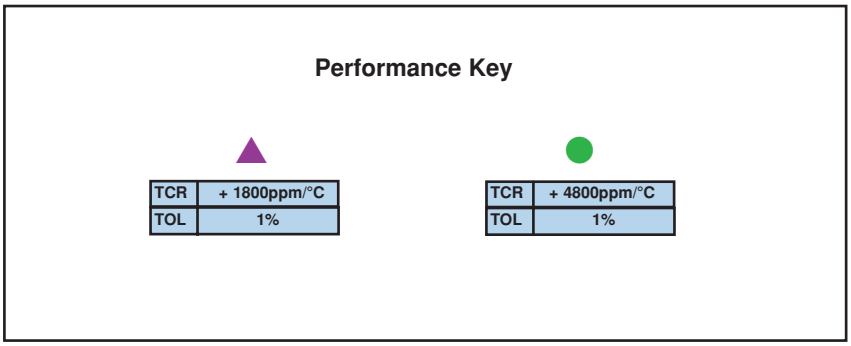
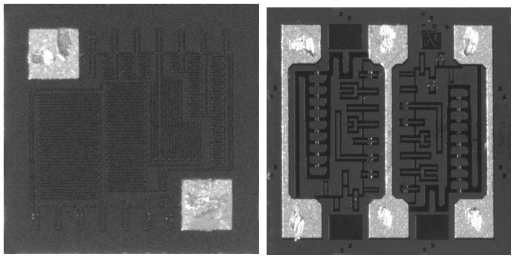
Thin Film High TCR Sensor (Wire Bondable Top Contact)





High TC Thin Film Resistors



Product may not be to scale

The RT resistor chip series offers high TC for special temperature sensing applications.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The RTs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- Small chip size
  0.020 x 0.020 inch - Format A
  0.030 x 0.030 inch - Format B
- Silicon substrate
- Large change in resistance over temperature
- Standard resistance ranges: 51Ω to 24kΩ - Format A
  51Ω to 51kΩ - Format B

APPLICATIONS

Vishay EFI RT chip resistors provide high TCR for circuit temperature compensation and are ideally suited for prototyping.

Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

WV (DC) VALUES AND TOLERANCES	
Tolerances	± 1%, ± 2%, ± 5%, ± 10%
RETMA Values	51Ω - 24kΩ - Format A 51Ω - 51kΩ - Format B

STANDARD ELECTRICAL SPECIFICATIONS	
PARAMETER	
Noise, MIL-STD-202, Method 308	- 20dB typical
TCR Absolute	+ 1800ppm/°C - Type 1 - Nickel + 4800ppm/°C - Type 2 - Palladium
TCR Linearity	< 3ppm/°C
Stability, 1000 hours, + 125°C, 25mW	± 1.0% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202 Method 107, Test condition F	± 0.5% maximum ΔR/R
High temperature exposure ± 150°C, 100 hours	± 0.50% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at 150°C)	65mW maximum - Format A 125mW, maximum - Format B
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.5% maximum ΔR/R

HIGH TCR SENSOR

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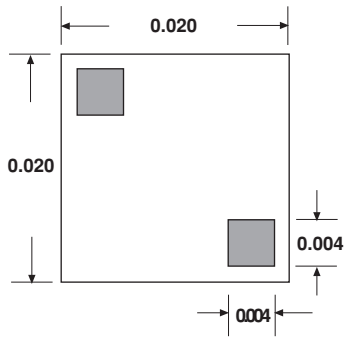
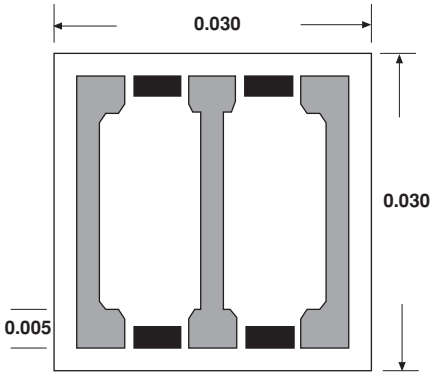
CONFIGURATIONS in inches

FORMAT A



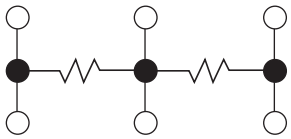
FORMAT B



STANDARD RTB AND RTD CONFIGURATIONS
Six locations. All pads 0.005 x 0.005 inches minimum

SCHEMATICS

$R_T = R_A + R_B$



MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size - Format A Chip size - Format B	0.020 x 0.020 ± 0.003 (0.5 x 0.5 ± 0.08mm) 0.030 x 0.030 ± 0.002 (0.762 x 0.762 ± 0.05mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Bonding pad size	0.004 x 0.004 (0.10 x 0.10mm) minimum
Pad material	15kÅ minimum Gold standard
Backing	None

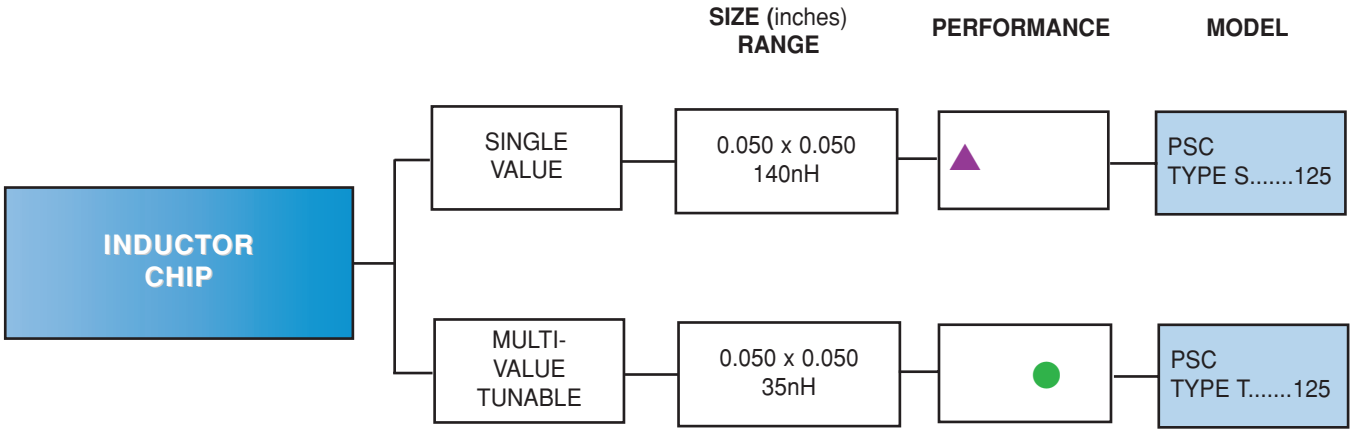
OPTIONS: Gold back for solder die attach

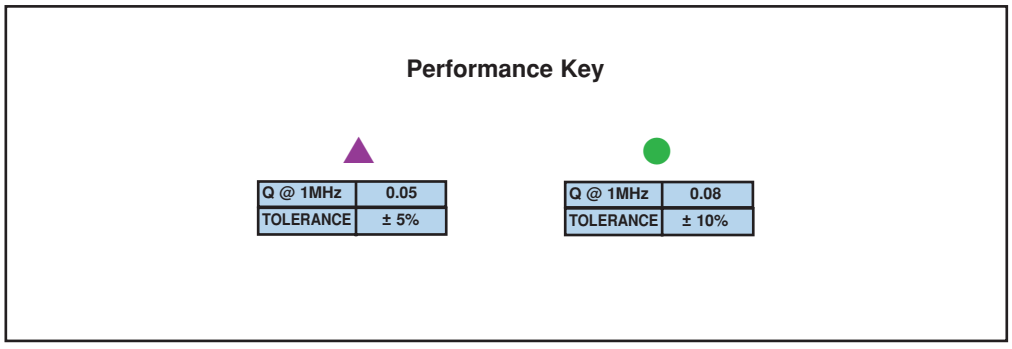
ORDERING INFORMATION

Example: 100% visualled, 100Ω, ± 10%

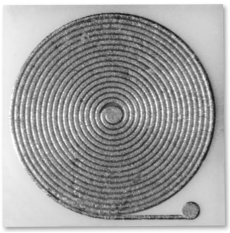
P/N:	W	RTB	XXX	1000	A	K
	INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
	W = 100% visually inspected parts in matrix tray per MIL-STD-883 **X** = Sample, commercial visually inspected parts loaded in matrix trays (4% AQL)	RTD - 30 RTB - 30 RTA - 20	Dependent on TC Consult factory 100 = + 1800ppm°C 300 = + 4800ppm°C	Use first 4 significant digits of the resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100	**F** = 1.0% **G** = 2.0% **J** = 5.0% **K** = 10%

Thin Film Inductor (Wire Bondable)





Spiral Chip Inductor



Product may not be to scale

FEATURES

- Small chip size: 0.050 inches square
- Alumina substrate
- Inductance up to 150nH
- Inductor material: thin film gold

The PSC Chip Inductors offer the best combination of size and value available. Generally custom built to specific value requirements, two versions are offered here.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The PSCs are 100% electrically tested for inductance and Q.

APPLICATIONS

Primary application is in microwave circuits as resistant element or as choke in power supplies. High self-resonance is important for choke applications and achieved by reducing capacitance between turns by physically increasing space between spiral lines. Multi tap coils are available for wire bond tuning but since inductors are very sensitive to pattern width/spacing and metallization thickness almost all are custom built to specification desired.

VALUES AND TOLERANCES

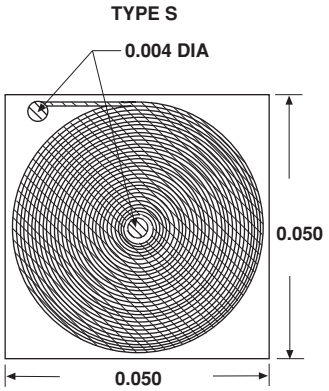
	TYPE S Single Bond	TYPE T Tunable
Q @ 1MHz	0.05	0.08
Tolerances	± 5% to ± 25%	± 10% to ± 25%
Steps		3 x 9%

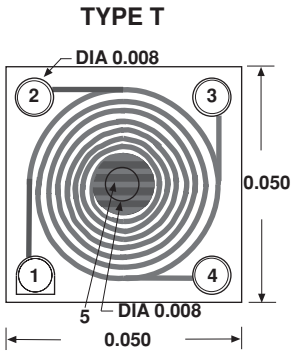
Custom values/sizes available. Quartz substrate available for higher Q.
Consult Application Engineer

STANDARD ELECTRICAL SPECIFICATIONS

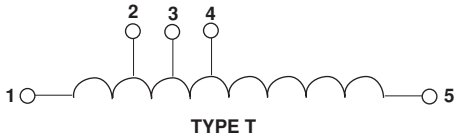
PARAMETER	
Operating temperature range	- 55°C + 125°C
Dielectric constant	9.8 for alumina
Coil resistance	< 5Ω
Insulation resistance	10^{12}Ω minimum

CONFIGURATIONS in inches





SCHEMATIC



MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.050 x 0.050 ± 0.003 (1.32 x 1.32 ± 0.076mm)
Chip thickness	0.015 ± 0.002 (0.38 ± 0.05mm)
Chip substrate material	99.6 Alumina, Quartz available
Bonding pad size	TYPE S 4 mil diameter typical TYPE T 8 mil diameter typical
Pad material	Gold

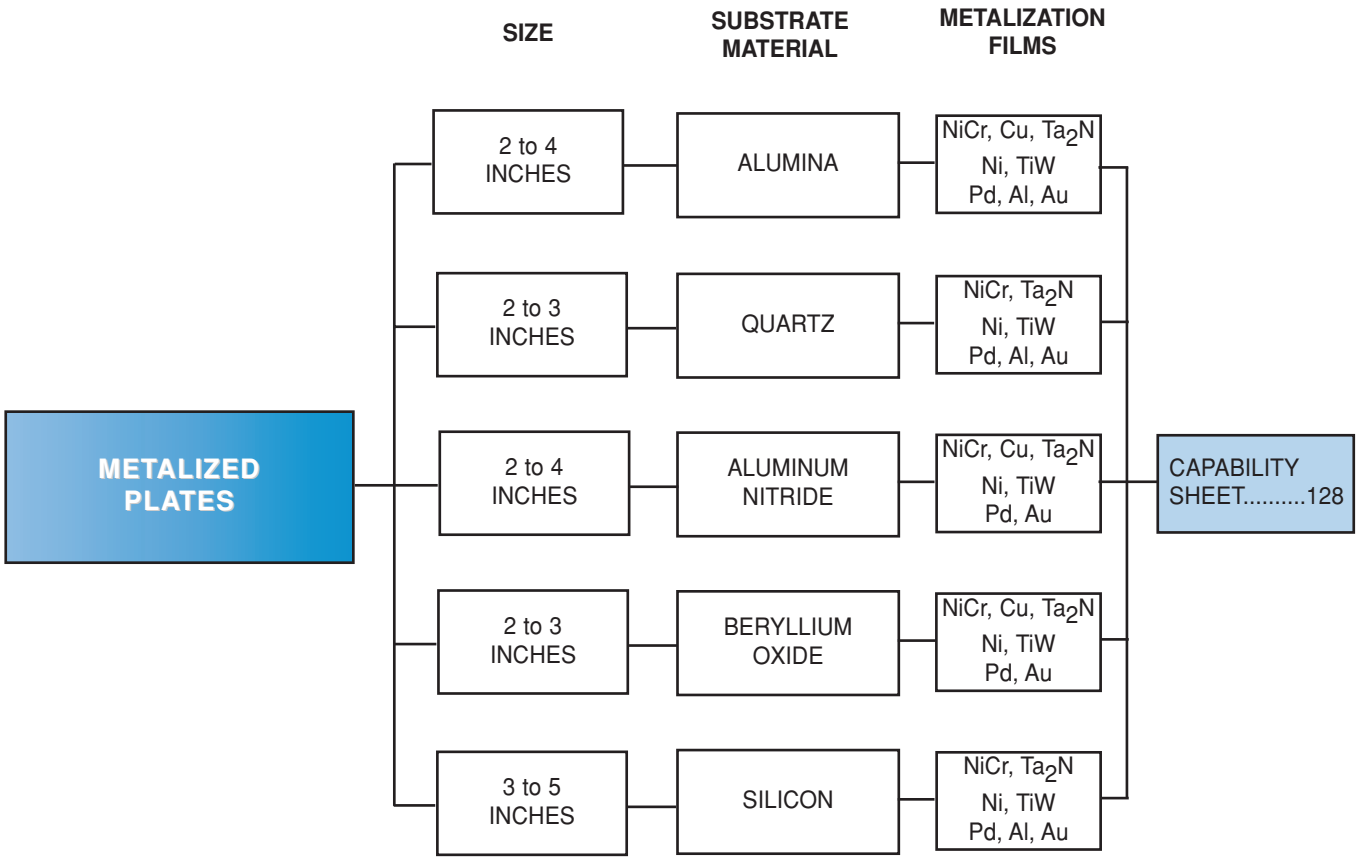
CHIP INDUCTOR

ORDERING INFORMATION

Example: PSC TYPE S, 140nH, ± 10%

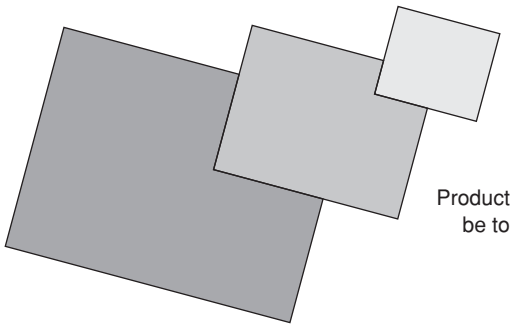
P/N: PSC	S/T	140	0	K
	TYPE	INDUCTANCE VALUE 3 significant digits	MULTIPLIER CODE **B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10	TOLERANCE CODE **J** = 5.0% **K** = 10% **M** = 20% **L** = 25%

Thin Film Metalized Plates



METALIZED WAFERS

Metalized Plates



Product may not be to scale

Vishay Electro-Films (EFI) offers the widest variety of metalization options, substrate materials, surface finishes and through hole metalization with rapid high volume delivery.

FEATURES

- Metalization on 1, 2, or 6 surfaces
- Excellent adhesion to all materials
- Sizes to 4 inches x 4 inches
- Metalized through holes with excellent adhesion
- Polished or “As Fired” surfaces
- High volume
- Rapid delivery

Unique, proprietary sputtering systems provide high volume and uniform deposition for up to three different metalization layers on one or both sides without breaking vacuum. This insures excellent adhesion to the surfaces and on the metalized thru-hole walls.
Volume plating with the conditions precisely controlled for each substrate insures uniform plating thickness from substrate to substrate as well as across individual substrates.

SUBSTRATE MATERIALS

Alumina, 99.6%

- Thickness - 0.010 inches, 0.015 inches, 0.025 inches
- Surface finish - as fired, 2 -4 microinches Polished, < 2 microinches
- Loss factor: 0.0004 typical @ 25°C - 1MHz
- Dielectric constant: 9.8 typical @ 25°C - 10GHz

Beryllium Oxide, Aluminum Nitride

- For high thermal conductivity requirements
- Metalized, patterned, with resistors

Quartz

- For low dielectric constant applications
- Very low noise amplifiers
- Consistently high adhesion levels

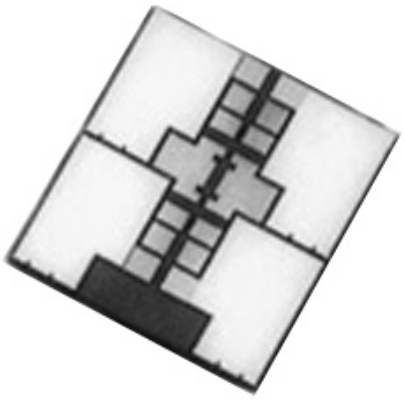
METALIZATION

The Vishay EFI sputtering systems employ long life (15 year), large area targets that provide consistent resistance, TCR and long term stability characteristics from plate-to-plate and run-to-run. You can be sure that all parts shipped for decades will have the same characteristics as the qualification run.

- Sputtered resistance material, 10Ω/square to 200Ω/square
- High stability nichrome.
- Moisture resistant tantalum nitride.
- Sputtered adhesion or barrier metal layers: NiCr, Ti, TiW, Ta2N, Mo, Cu, Ni, Pd.
- Plated layers to 1000 microinches: Ni, Cu, Au.

Ordering Information; Consult Application Engineer

High-Power Multi-Tiered Conductor Hybrid Circuit Substrate



Product may not be to scale

FEATURES

- Copper power lines up to 5000 microinches thick
- Gold small signal lines ± 100 microinches width tolerance
- Temperatures to 350°C
- Substrate material: Alumina, Beryllium Oxide or Aluminum Nitride
- Excellent adhesion
- Metallized through holes
- Filled vias
- Resistors available
- Sizes up to 4 inches x 4 inches

Vishay Electro-Films (EFI) has developed a thin film process that has the unique capability of incorporating up to 5000 microinches thick plated copper conductors on the same substrate with standard 100 to 300 micro-inch thick conductors.

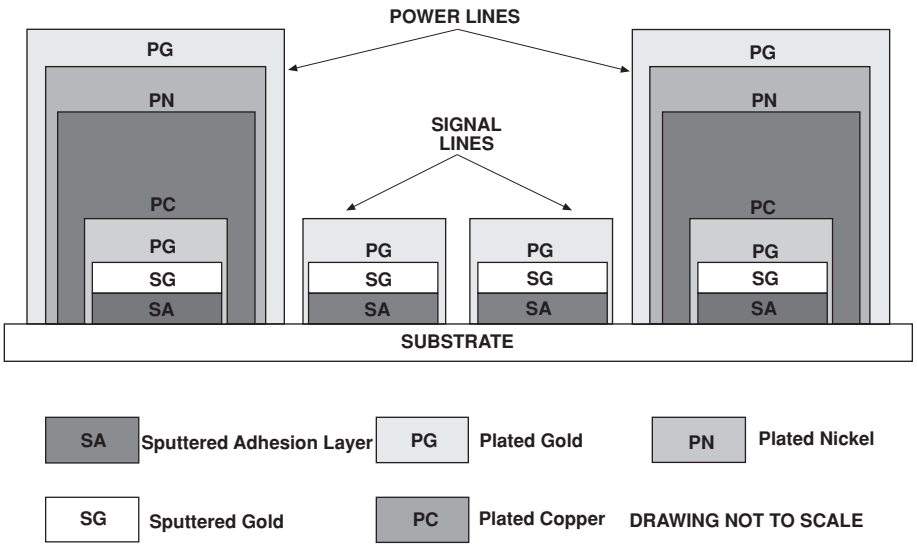
Some hybrid circuit applications require thick copper conductors for the power lines but standard thickness small signal lines to maintain tight line width control of critical elements. For example, a microwave application may require high power bias current to GaAs or other semiconductor devices while also requiring tight line width control to obtain good high frequency performance for lange couplers, filters or other critical signal patterns.

For standard, high power, low frequency hybrid circuit substrates, thick copper plating alone is ideal. The 5000µ inch thick plated copper has a resistivity of less than 0.15 milliohms/square.

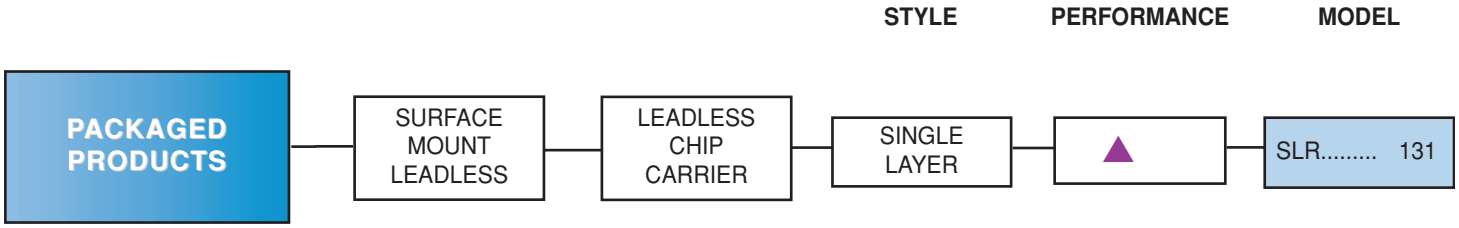
In most cases, the dc or low frequency copper power lines are overplated with nickel and gold to prevent oxidation, permitting high temperature processing and operation. The conductor material for the small signal lines is normally gold. Several substrate materials and various adhesion metals are available.

Consult Applications Engineer to discuss your requirements in detail to jointly develop the optimum metalization structure for your application.

TYPICAL CROSS SECTION



Thin Film Packaged Product Networks



Performance Key

▲	■	●	◆
TCR ± 10ppm/°C	TCR ± 25ppm/°C	TCR ± 50ppm/°C	TCR ± 100ppm/°C
TOL ± 0.05%	TOL ± 0.1%	TOL ± 0.2%	TOL ± 1%

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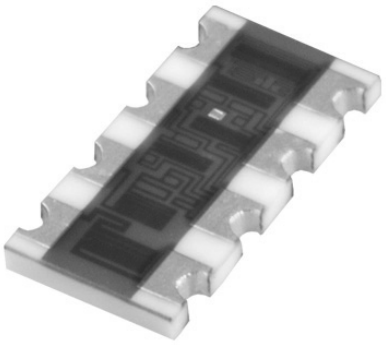
Single Layer Resistor Carrier Networks



Product may not be to scale

FEATURES

- Standard sizes 0.100, 0.150, 0.210 wide
- Custom sizes up to 0.500 inches x 0.500 inches
- Pad count to 36
- Mixed values to 500KΩ
- Multiple reference resistor groups
- Ratio tolerance to ± 0.01%
- Ratio TCR's to ± 1ppm/°C
- Nichrome resistor material standard. Tantalum nitride available, consult factory
- Custom pad spacing 0.025 inches or greater

SLR (Single Layer Resistor Carrier) networks are offered to provide the user with a leadless device that maximizes board density while maintaining tight ratio tolerances and TCR tracking. Pads are provided top and bottom connected by edge castellations for ease of visual solder joint inspection. Resistors can be covered with Vishay Electro-Films (EFI) proprietary thermal set plastic for physical protection or left uncoated to facilitate user trimming.
SLR's are provided with 0.050 inches standard contact spacing; however, 0.025 inches contact spacing is also available. The standard contact metallization is gold flash over nickel plate. Solder coated contacts can be provided if preferred. Custom configurations, values, and tolerance combinations are available with fast turnaround.

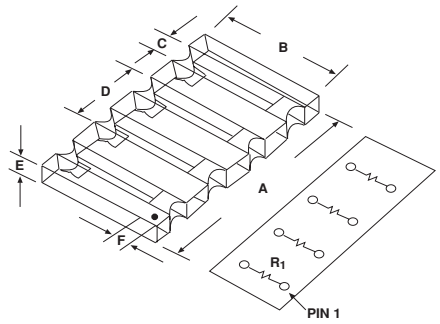
PRODUCT CAPABILITIES	
Resistance Range	10Ω to 500KΩ
Absolute Resistance Tolerance	± 1% to ± 0.05%
Resistance Ratio Tolerance	± 0.1% to ± 0.01%
Absolute TCR	± 50ppm/°C; available to ±10ppm/°C
Ratio TCR	± 5ppm/°C; available to ±1ppm/°C
Absolute Resistor Stability (Mean)*	300ppm/1000hours @125°C (typical)
Ratio Resistor Stability (Mean)*	18ppm/1000hours @ 125°C (typical)
Package Power Dissipation	100mW/Res @70°C, 50 mW/ 125°C
Temperature Range	0°C to + 70°C, - 40°C to + 85°C, - 55°C to + 125°C

The SLR construction allows for a wide selection of special sizes and shapes with rapid turnaround and low NRE costs. The holes for the edge castellations are laser drilled into a multiple-up, large area substrates in-house prior to metallization. This permits new configurations with only laser software and a mask set.

Custom parts can be provided with combinations of features listed:

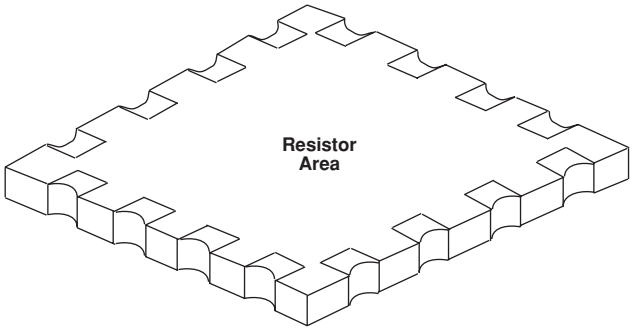
1. Any combination of resistor values between 100Ω and 100KΩ in the standard sizes.
2. Custom resistor network patterns (no crossovers).
3. A wide variety of rectangular sizes and shapes with contact pads on two to four sides.
4. Pad center-to-center spacings from 0.025 inches (0.635 mm) and larger.
5. Uncoated to permit customer trimming.

OUTLINE DRAWING

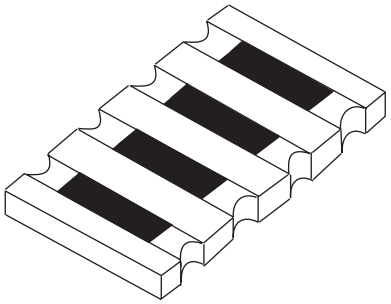


DIMENSIONS in inches [millimeters]						
Centers	**A**	**B**	**C**	**D**	**E**	**F**
0.025	*	0.100	0.015	0.025	0.015	0.020
[0.64]	*	[2.54]	[0.38]	[0.64]	[0.38]	[0.51]
0.050	**	0.100	0.030	0.050	0.015	0.020
[1.28]	**	[2.54]	[0.76]	[1.28]	[0.38]	[0.51]
0.050	**	0.150	0.030	0.050	0.025	0.020
[1.28]	**	[3.84]	[0.76]	[1.28]	[0.64]	[0.51]
0.050	**	0.210	0.030	0.050	0.025	0.020
[1.28]	**	[5.37]	[0.76]	[1.28]	[0.64]	[0.51]

* 0.025 inches [0.64mm] per resistor, 2 to 18 pads.
** 0.050 inches [1.28mm] per resistor, 2 to 18 pads.



Single Layer 16 Pin Chip Carrier
Chip measures 0.300 inches x 0.300 inches.
Castellations are on 0.050 inches (1.27mm) centers.
(Special Order)



Standard Pitch: Castellations are
on 0.050 inches (1.27mm) centers
(0.025 inch pitch special order)

ORDERING INFORMATION

Example: SLRC-4-10000-1-B-F-D-C-G, 8 Lead 0.100 wide, with 4 Identical 100KΩ Isolated Resistors, Absolute Tolerance: 0.1%, Ratio Tolerance: 0.1%, Absolute TCR: 50ppm/°C, Ratio TCR: 2ppm/°C, Gold Termination

SLR MODEL	**C** WIDTH	**4** NUMBER OF RESISTORS	**10000** RESISTANCE VALUE	**1** VALUE MULTIPLIER %	**B** ABSOLUTE TOLERANCE %	**F** RATIO TOLERANCE	**D** ABSOLUTE TCR. PPM/°C	**C** RATIO TCR PPM/°C	**G** TERMINATION
	C = 100 **N** = 150 **M** = 210		ALL SAME VALUE (5 Significant Digits)	**C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1.0 **1** = 10.0 **2** = 100.0	**A** = 0.05 **B** = 0.1 **C** = 0.2 **D** = 0.5 **F** = 1.0 **G** = 2.0 **J** = 5.0 **K** = 10.0 **M** = 20.0	(To R1) **A** = 0.005 **B** = 0.010 **C** = 0.025 **D** = 0.050 **F** = 0.100 **H** = 0.250 **J** = 0.500 **K** = 1.000 **X** = N/A	**A** = 10 **B** = 25 **D** = 50 **E** = 100	**B** = 1 **C** = 2 **D** = 3 **F** = 5 **G** = 10 **X** = N/A	**G** = Ni/Gold **S** = Solder Coated

NOTE: Factory will covert order number into final part number.
For special value combinations and pin outs consult Application Engineer

Resistor Network Time Stability Curves

NiCr on Alumina, 125°C

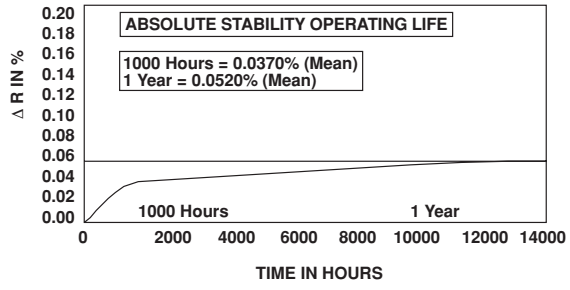


Figure 1

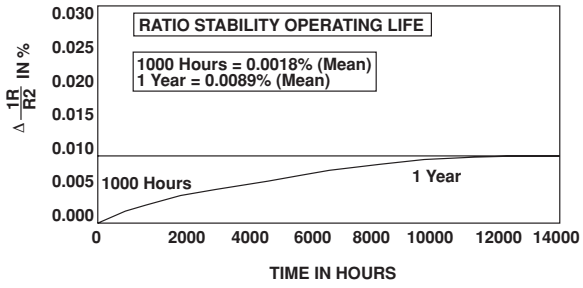


Figure 2

NiCr on Alumina, 200°C

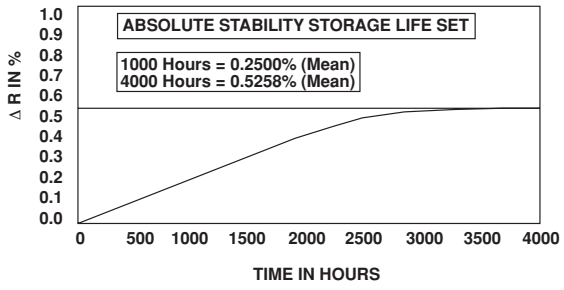


Figure 3

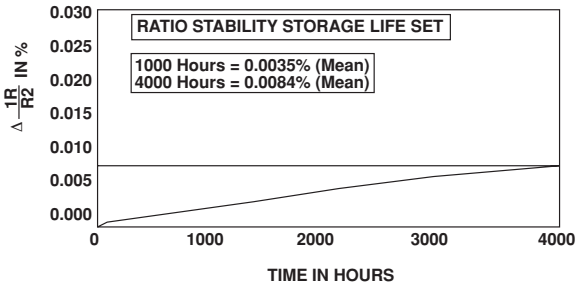


Figure 4

Ta_2N on Silicon, 125°C

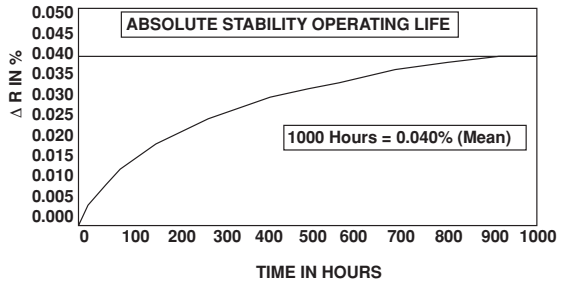


Figure 5

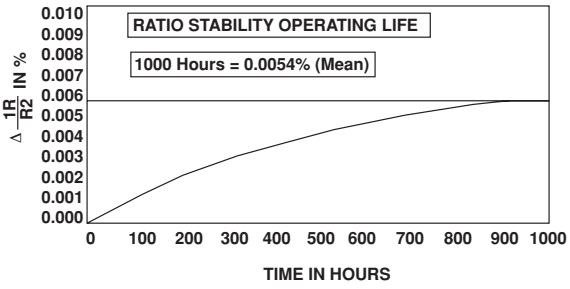


Figure 6

NiCr on Alumina

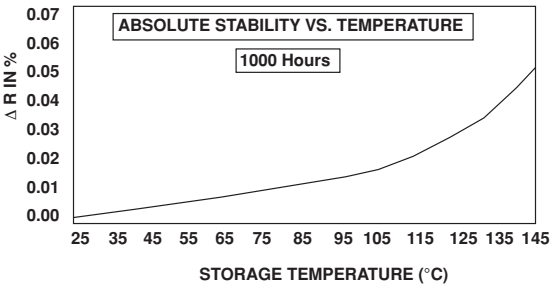


Figure 7

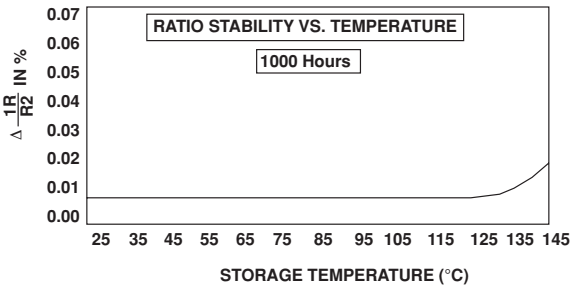
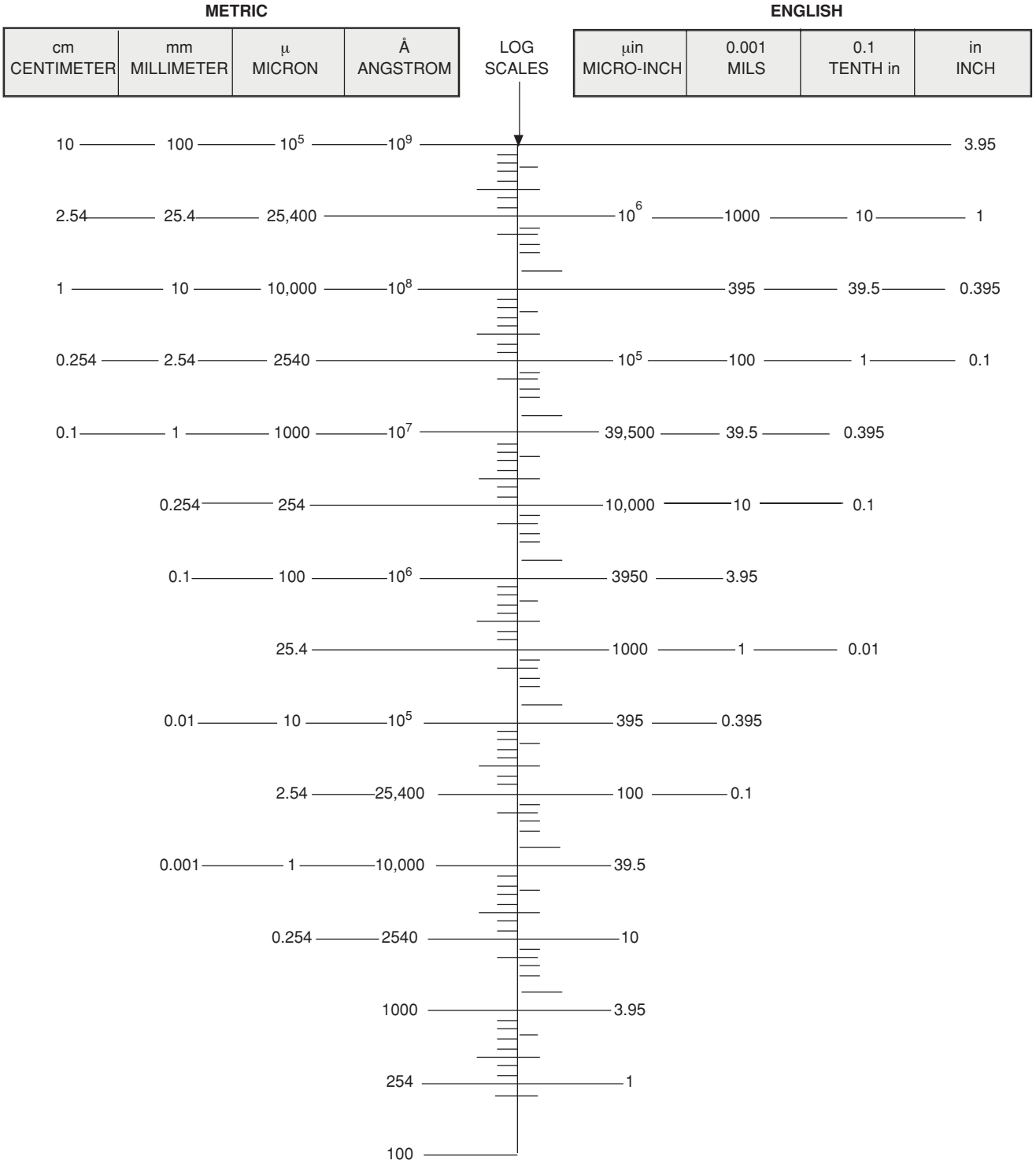


Figure 8

Thickness Conversion Chart



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